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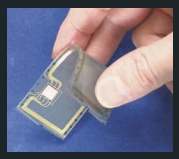

FIBRE CHANNEL, INFINIBAND, ETHERNET:

WHICH INTERFACE WILL GET TRACTION?

Page 58

CAT5 TRACKS:AUDIO GOES THE DISTANCE, RELIABLY AND ON TIME
Page 47

STRUCTURED ASICs DESERVE SERIOUS ATTENTION AT 90 NM
Page 69

WINDOWED-WATCHDOG TIMERS ENHANCE SYSTEM SECURITY
Page 79

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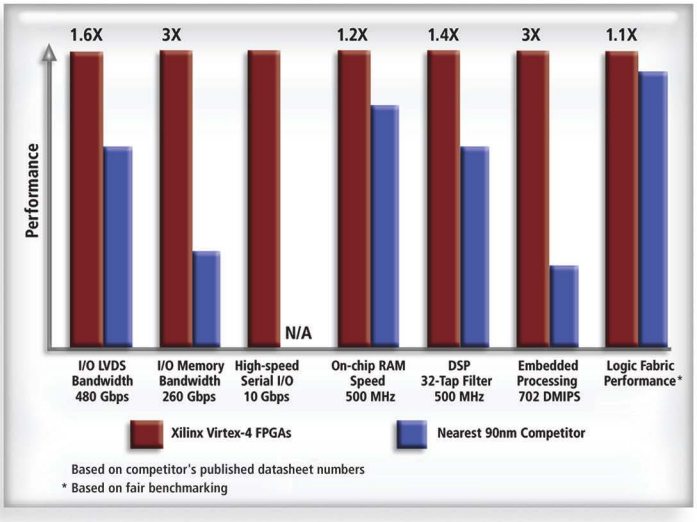

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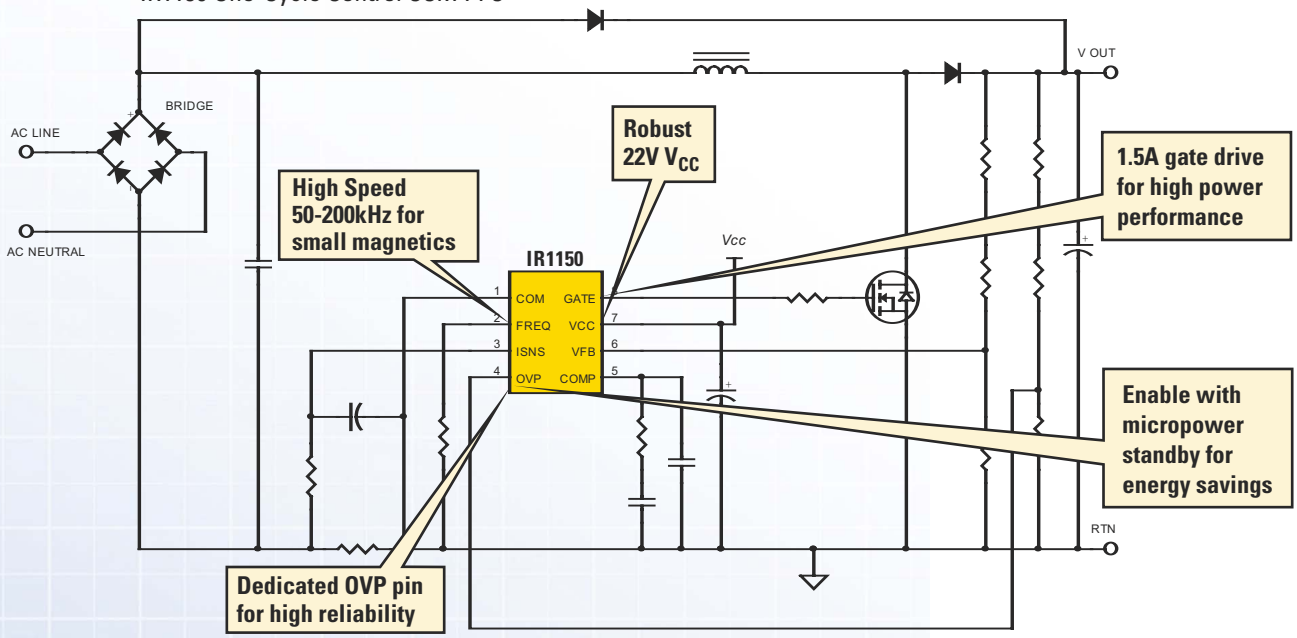

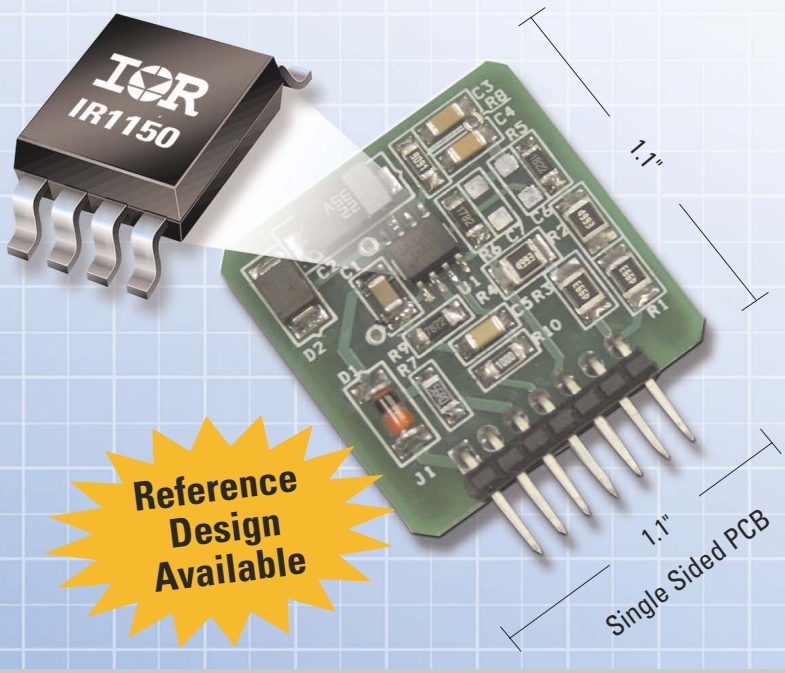

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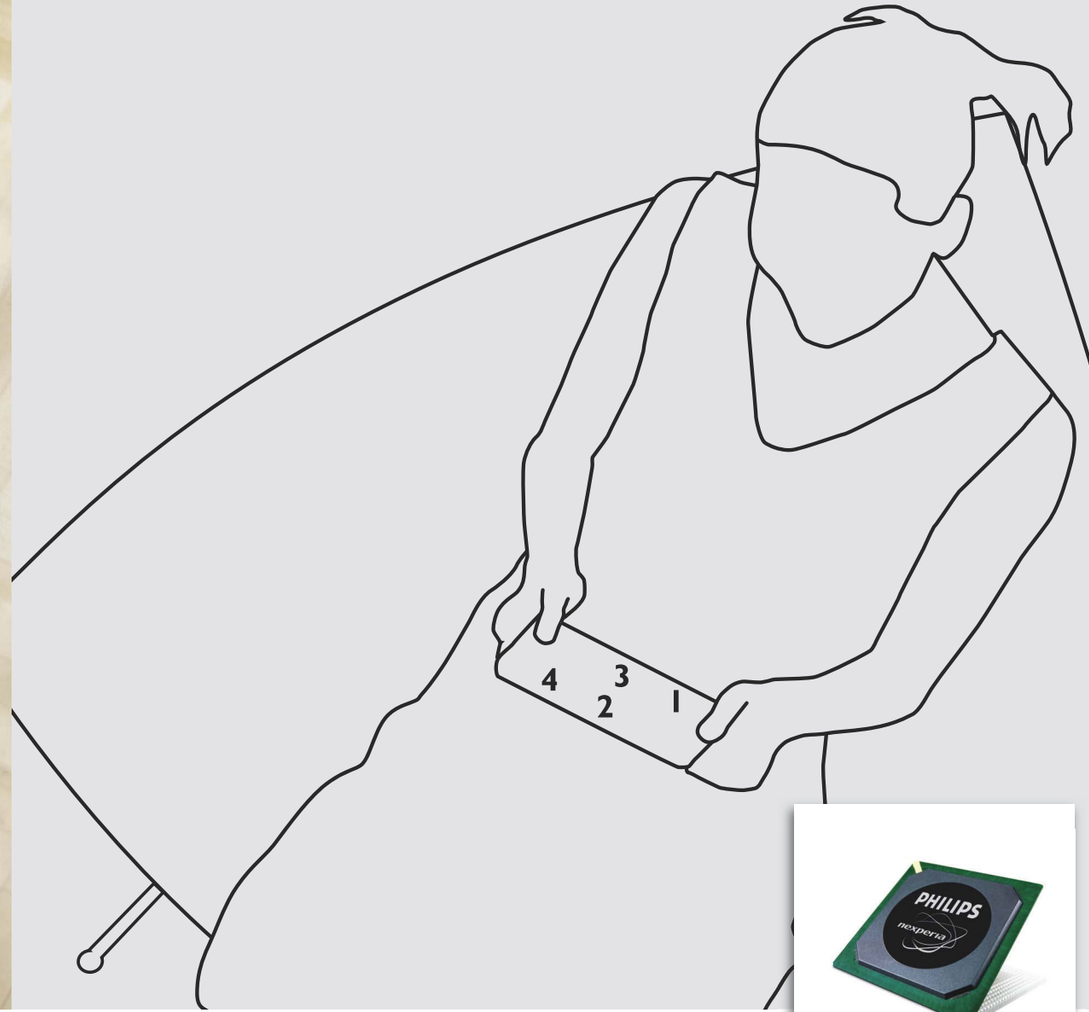

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2. **Power Management Unit –** PCF50606 PMU+. One chip provides complete system power supply and management including DC/DC converters, battery management, charger control and dynamic power control that optimizes multiple voltage levels in real time to minimize power consumption.
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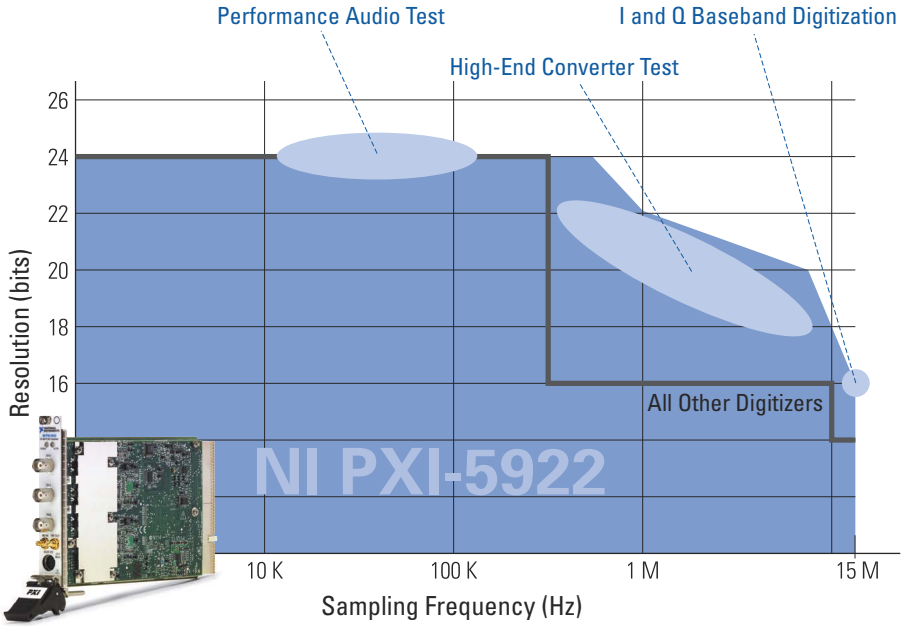

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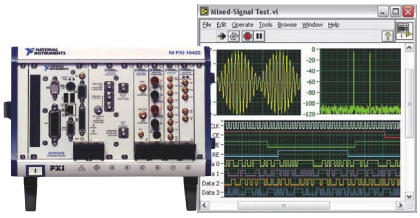

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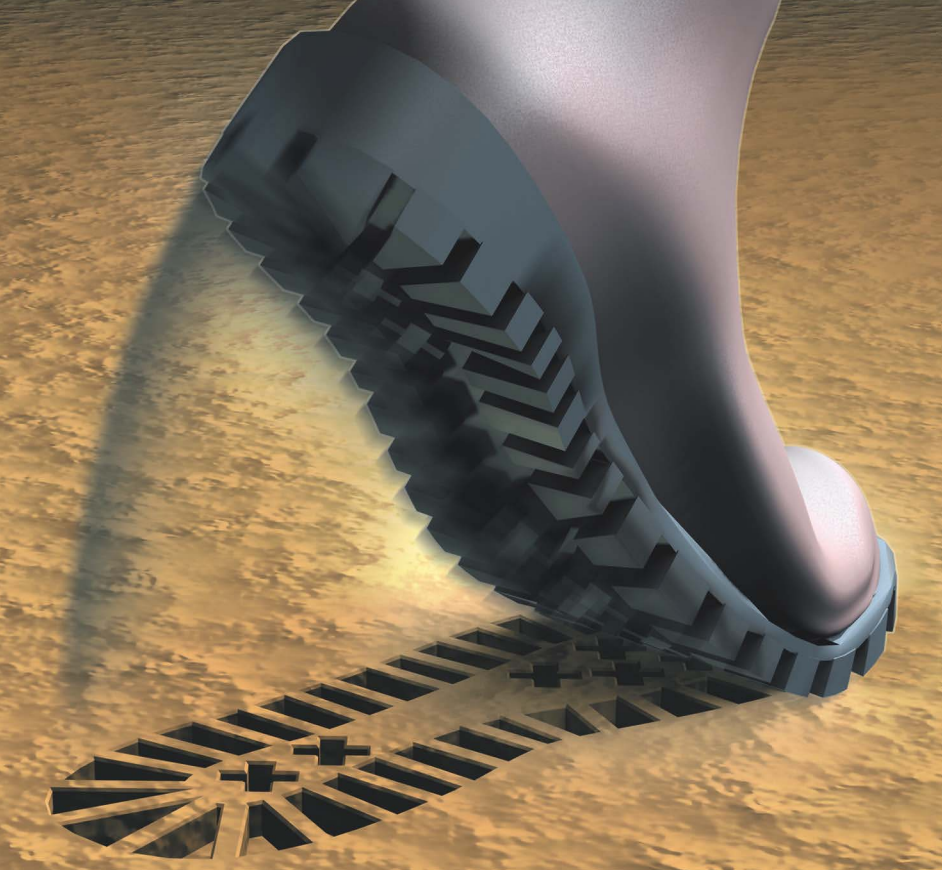

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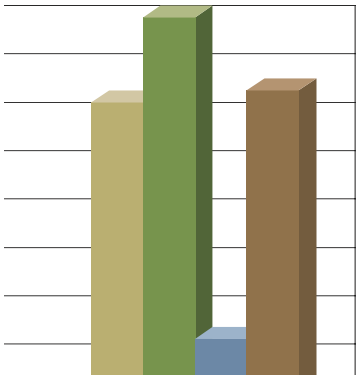

Which interface will get traction?

by Maury Wright, Editor at Large

CAT5 tracks: Audio goes the distance, reliably and on time

by Brian Dipert, Technical Editor

Structured ASICs deserve serious attention at 90 nm

by Michael Santarini, Senior Editor

Windowed-watchdog timers enhance system security

by Donald W Corson, EM Microelectronic

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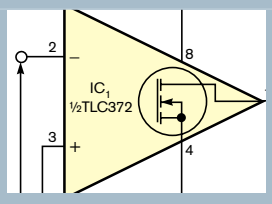

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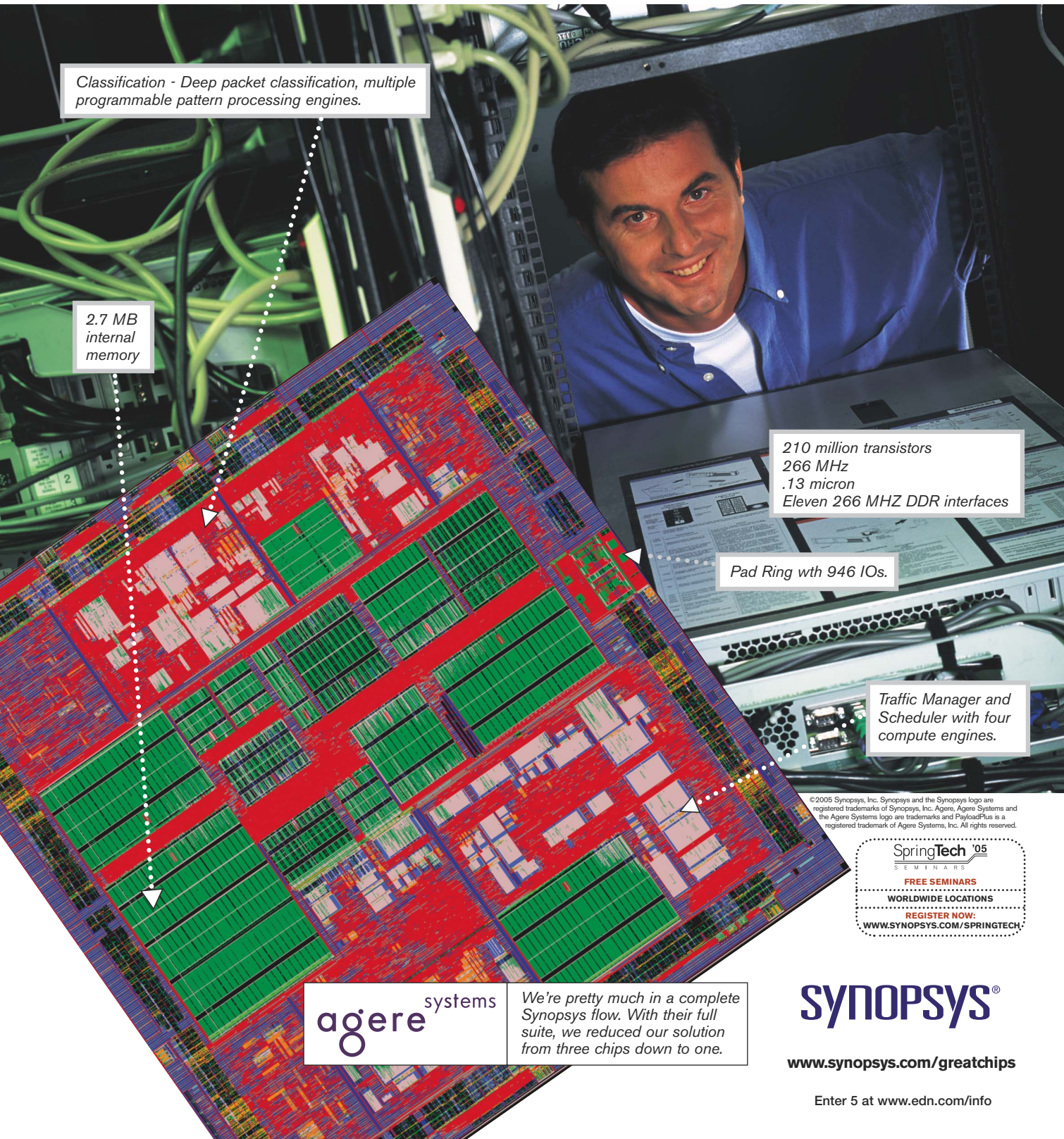

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*According to research by TDK, June 1, 2005

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TDK

BY BILL SCHWEBER, EXECUTIVE EDITOR

Are we losing our innovation religion?

If you really want to worry about the state of our industry—for both our engineers and our companies—pick up a copy of the March 21, 2005, *Business Week*, which is available free online with registration or at your local library. The multifaceted cover story "Outsourcing Innovation" filled in the details with examples and numbers of what many of us already know or have heard: Not only engineering-design roles, but also all of the functions—the very essence of many companies—are "going away." We are helping them to evaporate.

This issue is not about simple globalization. Globalization itself—locating your staff worldwide to take advantages of various perceived attributes they offer, for both technical expertise and lower cost—is unavoidable given the time, cost, complexity, and pressures of today's designs. Also, globalization provides an around-the-clock advantage and the technology-enabled ease of transferring data and designs from Point A to Point B.

But why stop there, many companies are asking? You can outsource product design to a third party, which in turn may use big chunks of external IP (intellectual property); you can outsource physical manufacturing; and now, you can even outsource your research and development. The article gave plenty of examples of which companies are using this approach and the results in apparent cost (read "people") savings. What's left? Not to worry, many say: The companies that outsource so many aspects of their roles can do the upfront product definition, as well as the product marketing. Sounds like a plan, doesn't it?

Outsourcing innovation starts a dangerous downward spiral.

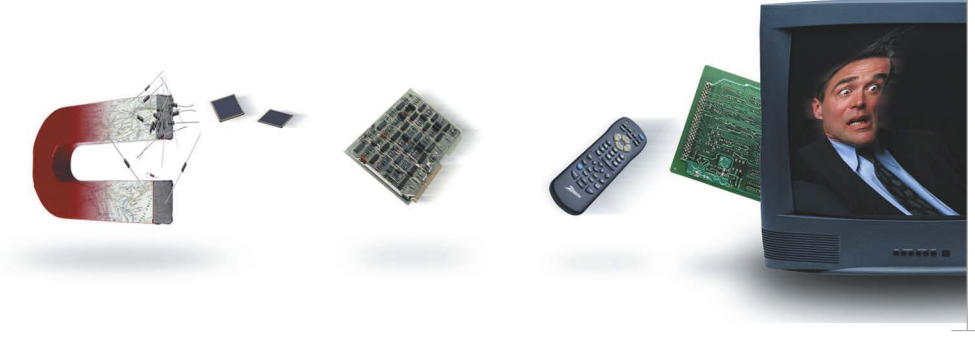
However, all this outsourcing buries a reality: Once your outsource partners learn how you define products, how you market them, and whatever other "secret" understanding you have or you assume that you have, and you have an "in" on your markets, those partners no longer need you. It's that simple. The "secret sauce" you think makes a difference may not be such a secret or maybe isn't the barrier to entry that you thought it was.

You already see this entry of new players in diverse markets, such as home appliances and consumer products. In these markets, companies most of us have never heard of are using widely available chip sets and components and quickly developing a significant presence in the markets of long-established market leaders.

If a company thinks it can survive and remain a market force if it just does marketing and branding, while abandoning true R&D, design, and innovation, the company is deluding itself. The shelves of Wal-Mart are full of brands that used to be real players and now exist only as nameplates.

Remember RCA? Once the undisputed leader in TV innovation, the company spent more than a billion in 1950s' dollars to develop color TV as we know it today, including architecture, CRTs, imagers, and much more. Then, in addition to its other corporate missteps, such as going to conglomerate mode and supplying home appliances, carpets, rental cars, and more, it began the process of shedding. It outsourced the labor-intensive soldering of the wired TV chassis that predate pc boards, albeit using US-sourced components. Next, the manufacturing of these components—mostly passives—moved; then, the design of these components traveled. Next came manufacturing of the more complex parts; then, their design; and, soon, all that was left was an empty shell of a well-respected brand, and a name that used to have distinctive value—but now had none.

When your functions and true added value have atrophied by that magnitude, anyone can step in and take away your markets, shelf space, and business. Today's smart move to outsourcing almost everything may be the dumbest long-term move a company can make. EDN



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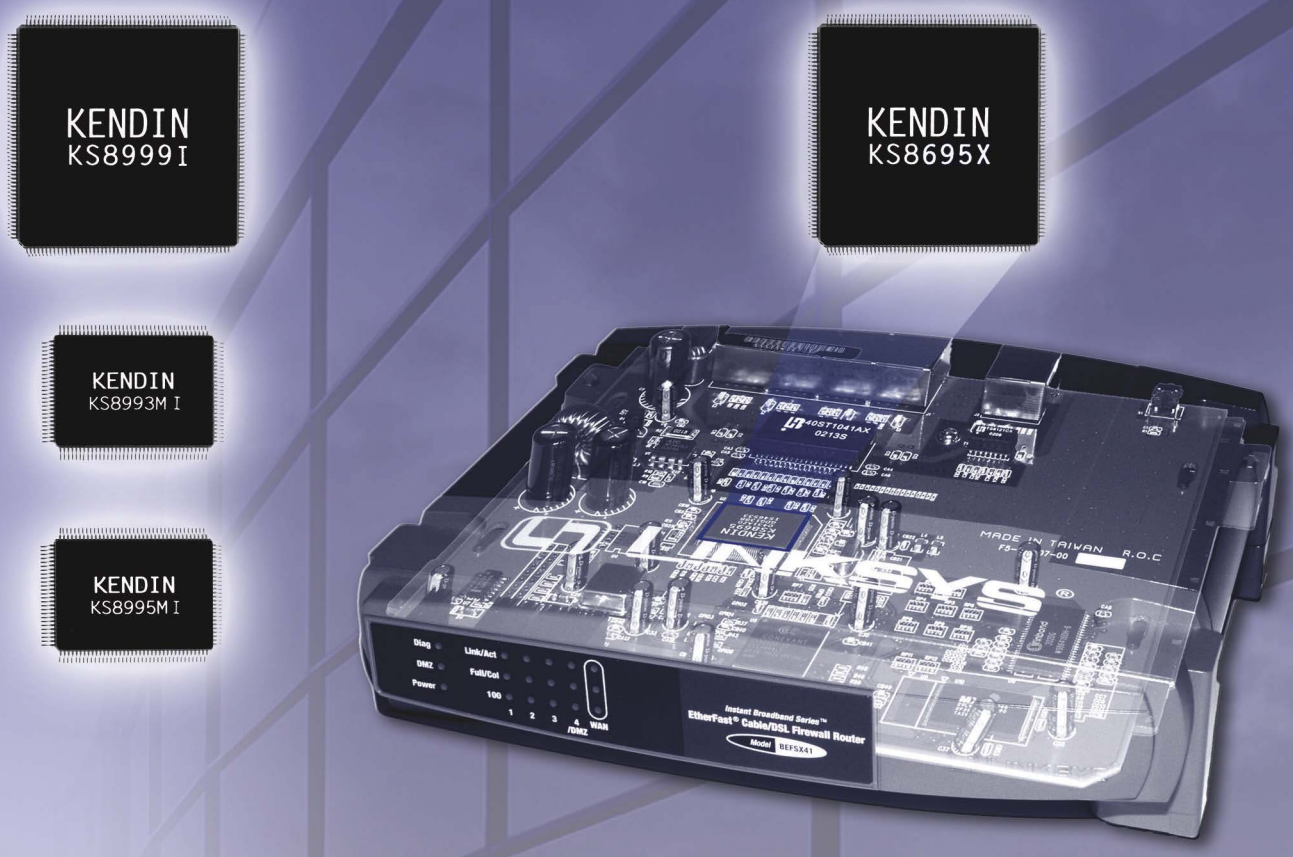

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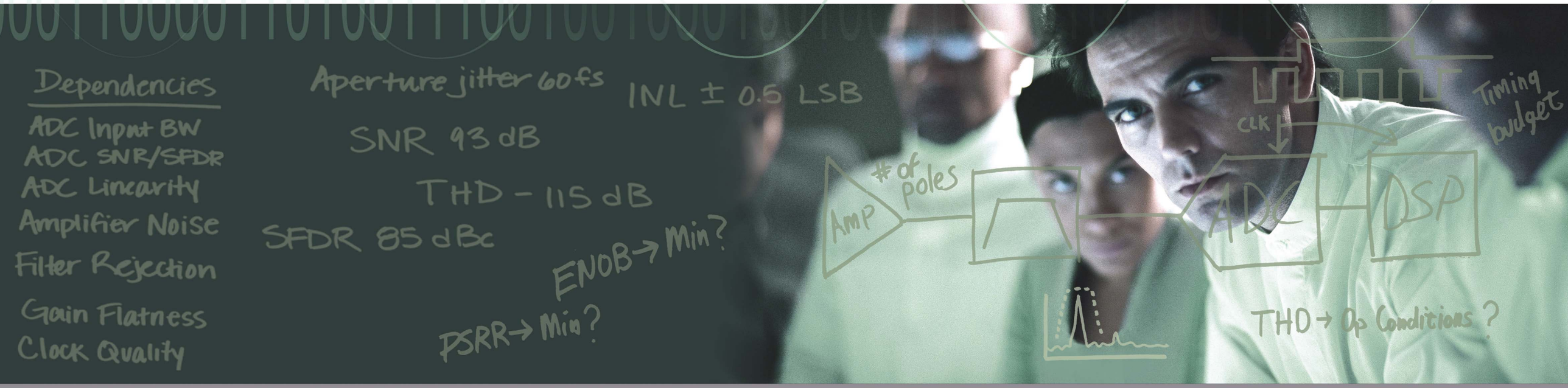
Reed Electronics Group

Breakthrough data converter performance beyond speed and bits.



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14 bits, 125 MSPS
80 dBc SFDR @ 300 MHz
60 fs aperture jitter

AD9446
16 bits, 100 MSPS
80 dBc SNR
90 dBc SFDR

AD7621
16 bits, 3 MSPS
±1 LSB INL
90 dB SNR

AD7641
18 bits, 2 MSPS
±2 LSB INL
93 dB SNR

AD7760
24 bits, 2.5 MSPS
−100 dB THD
100 dB to 118 dB SNR


Base Station


Test Gear


Instrumentation


CT Scanner


Data Acquisition

. . . where it matters most.

The performance levels that define your design

In the world of data conversion, more bits are good, and faster sample rates are even better. But good performance in one area is of little value if it comes with compromises in other areas, like ac linearity, dc accuracy, power consumption, integration, packaging, or price. Today, benchmark converters are about delivering leading performance on multiple levels and giving designers the combination of features they need for their particular applications. Like best-in-class nonlinearity for medical designs (AD7641), unparalleled SFDR for base stations (AD9445), or a combination of precision and small size (7 mm × 7 mm) for portable instruments (AD7621)—and of course, all with best-in-class speed and resolution to start.

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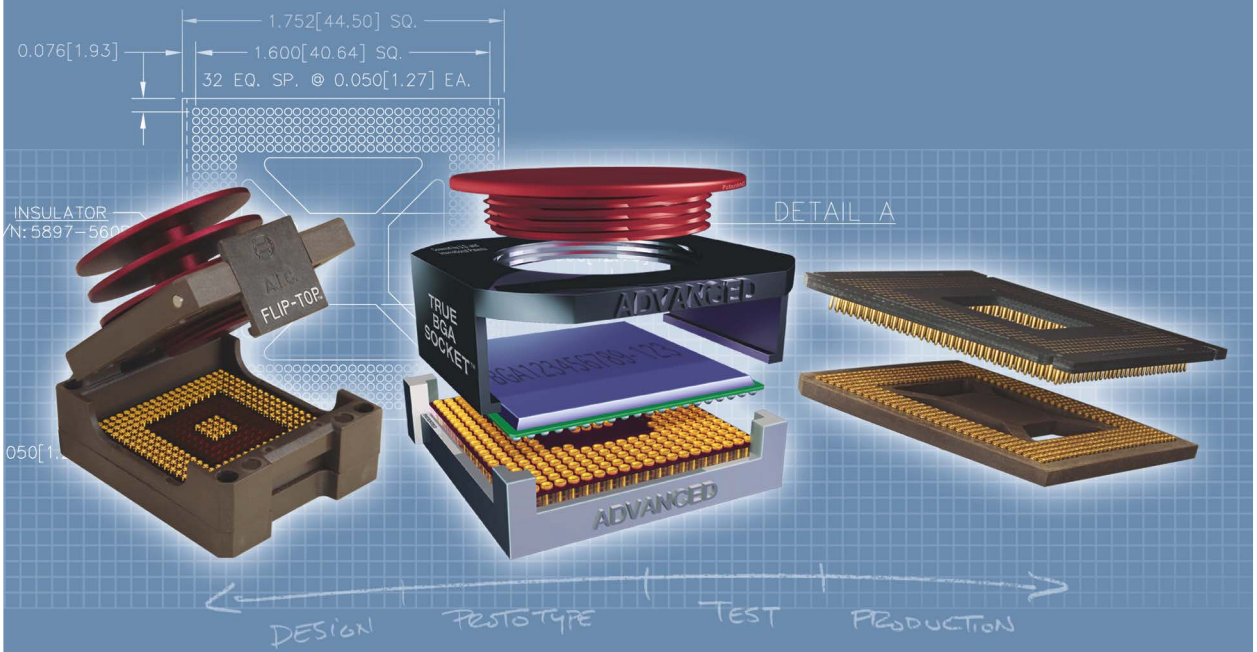
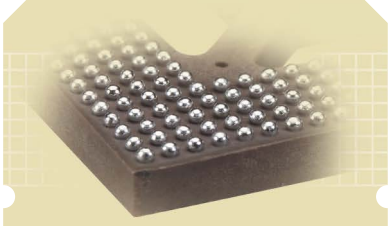


And Every Step In Between.

Products shown may be covered by patents issued and/or pending.



Standard Eutectic or Optional Lead-free

Advanced now offers select BGA sockets with lead-free solder ball terminals to comply with worldwide directives.

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS AND INNOVATORS

Intense LEDs take on the sun

LEDs are moving up the intensity scale for outdoor-signage uses, as the OVL series demonstrates. The devices are available in a range of colors and 3-, 4-, and 5-mm sizes.

According to Richard Saffa, vice president of visible LEDs at Optek Technology, the company's OVL series of LEDs performs in full sunlight for a variety of display and signage applications, including commercial outdoor advertising. The through-hole, oval LEDs, in 3-, 4-, and 5-mm sizes, are available in blue, green, red/orange, and red with intensities that vary depending on color and size. For example, the 5-mm, red, AlInGaP device has typical intensity of 950 mcd at 20 mA, and the green InGaN device has an intensity of 1750 mcd.

Viewing angle also depends on size; representative viewing angle is 50° at half-power and 110° maximum. Power dissipation for these 25-cent devices is approximately 130 mW.—by Bill Schweber

▷**Optek Technology**, www.optekinc.com.

Book leads those on the digital dark side to the analog force

A familiar name to *EDN* readers, Bonnie Baker takes many of the subjects and themes of her popular "Baker's Best" column into more detail and depth in *A Baker's Dozen: Real Analog Solutions for Digital Designers* (Newnes/Elsevier, ISBN 0-7506-7819-4, May 2005). This clearly written, highly readable book explains both basic topics, such as A/D-converter operation, and the dilemmas that designers face, such as where, when, and how to filter signals in the signal-processing chain. Other topics include the use and validity of Spice models; digital-versus-analog-processing trade-offs and cooperation; and noise, layout, and grounding.

The $59.95, 368-pg paperback devotes a chapter to the all-important topic of troubleshooting mixed-signal designs. Colleges don't teach this subject, but engineers usually teach themselves at the debugging bench at first using bad judgment, which leads to experience and then to good judgment. This self-teaching primer will enhance your design, decision, and debugging skills so that you can face the reality of mixed-signal systems or digital designs with their inevitable analog-world aspects.—by **Bill Schweber**

▷**Newnes/Elsevier**, http://books.elsevier.com.

FEEDBACK LOOP

"Did I read that right? You can program the DSP directly in Visual Basic? Somebody actually built a VB compiler that generates native DSP code? What's next? Programming a DSP in Cobol?"

Ken Dyck, in *EDN*'s Feedback Loop on www.edn.com/article/CA605784. Add your comments.

Simple transformer monitors ac currents

Is there an electrical component as versatile as the venerable transformer in its various manifestations? For measuring ac current, the 5600 series from C&D Technologies combines isolation to 500V with primary current rating to 10A. The device finds use in switched-mode power-supply feedback loops, motor-current monitoring, and other sensing applications. Bandwidth is 20 to 200 kHz, and these transformers are available in 50-, 100-, 200-, or 300-turn versions, for different sensitivity factors. Internal inductance is 5 to 335 mH, and dc resistance ranges from 117 mΩ to 8.6Ω.

The less-than-$1 units are available as two-lead and center-tapped devices and measure 16.8×20×8.9 mm.

—by Bill Schweber

▷**C&D Technologies Inc,** www.cd4power.com.

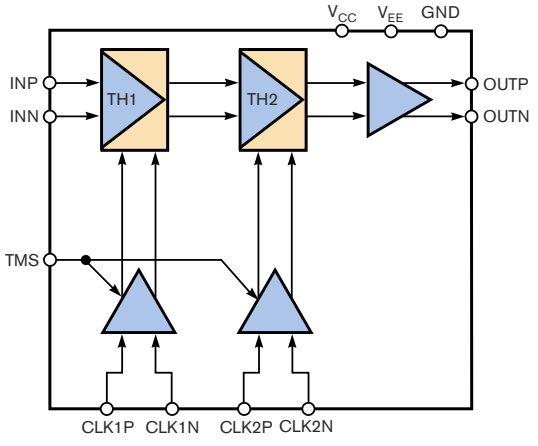
The 5600 current-sensing transformer series offer 500V-dc isolation in 50- to 300-turn versions.

Track-and-hold device allows direct capture of signals greater than 10 GHz

The extremely wideband RTH050 dual track-and-hold device from Rockwell Scientific enables direct conversion of gigahertz-range signals and signal edges with rise times of approximately 20 psec. This unit has small-signal input bandwidth of 15 GHz and supports a sampling rate of 100 to 1000M samples/sec. The differential signal-path device incorporates cascaded track-and-hold circuits to provide a hold time that is greater than one-half the clock cycle, which reduces bandwidth requirements for the subsequent signal-handling chain. Aperture jitter is 100 fsec, and acquisition time is 200 psec. Hold-mode distortion is −42 dB for a 5-GHz signal with 0.5V p-p amplitude, rising to −30 dB for a 7.5-GHz signal; noise is less than 1 mV. Spurious-free dynamic range is 65 dB with a 1.060-GHz, 0.5V p-p signal.

According to Ron Latreille, product-line manager for mixed-signal products, the improved speed of this unit, compared with its predecessors, allows users "to digitize a broader range of signals with no increase in power consumption" at 1.65W. A similar device, the RTH055, also integrates 12-dB attenuators to eliminate the need for external components to scale down signals with excessive full-scale magnitude. The RTH050 sells for $300 (100) and is available in a 13-lead HSD package.—by Bill Schweber

▷**Rockwell Scientific Co LLC**, www.rockwellscientific.com.



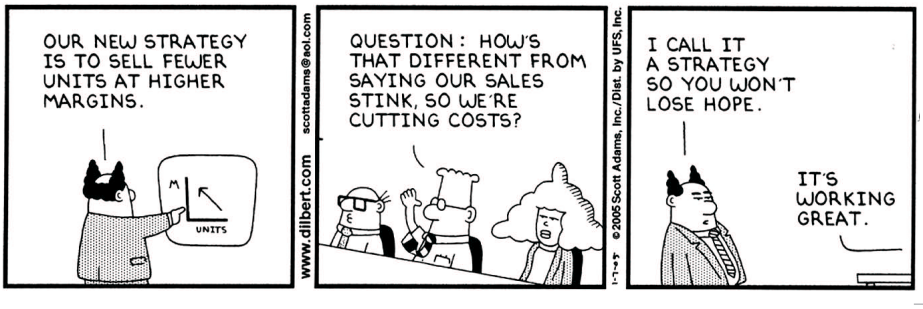
Simple in concept but fast in execution, the RTH050 track-and-hold device from Rockwell Scientific offers a 15-GHz bandwidth and a 1G-sample/sec sampling rate with a dual internal structure for relaxation of interface timing.

FEEDBACK LOOP

"The Nyquist Theorem addresses avoiding aliasing of a reconstructed signal, not perfectly reconstructing the original signal. For signals approaching one-half the Nyquist frequency, severe amplitude attenuation periodically occurs as the sampled points move into and out of phase with the signal."

Konrad Kratz, in *EDN*'s Feedback Loop on www.edn.com/article/CA529378. Add your comments.

DILBERT *By Scott Adams*



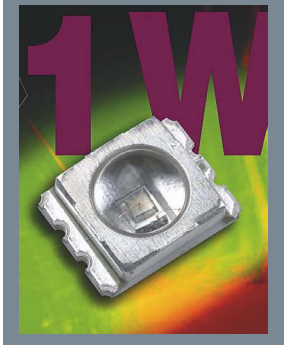
LED module delivers 60 lumens

07.07.05

BivarOpto's LK series encompasses single-chip, 1W LEDs targeting safety, signaling, emergency, and general illumination. The 465- to 635-nm surface-mount devices, also available in white to 8000K, use a Cree XLamp die that includes an aluminum pc-board base for managing thermal issues. The lead-free encased metal-core module, which measures 20.3 mm sq, includes an integral lens; you can also get a two-pin header-based connector for snap-in and ease of replacement. The LED operates from −30 to +100°C; maximum forward current is 400 mA. The LK series modules sell for $4 (volume quantities).

—by Bill Schweber

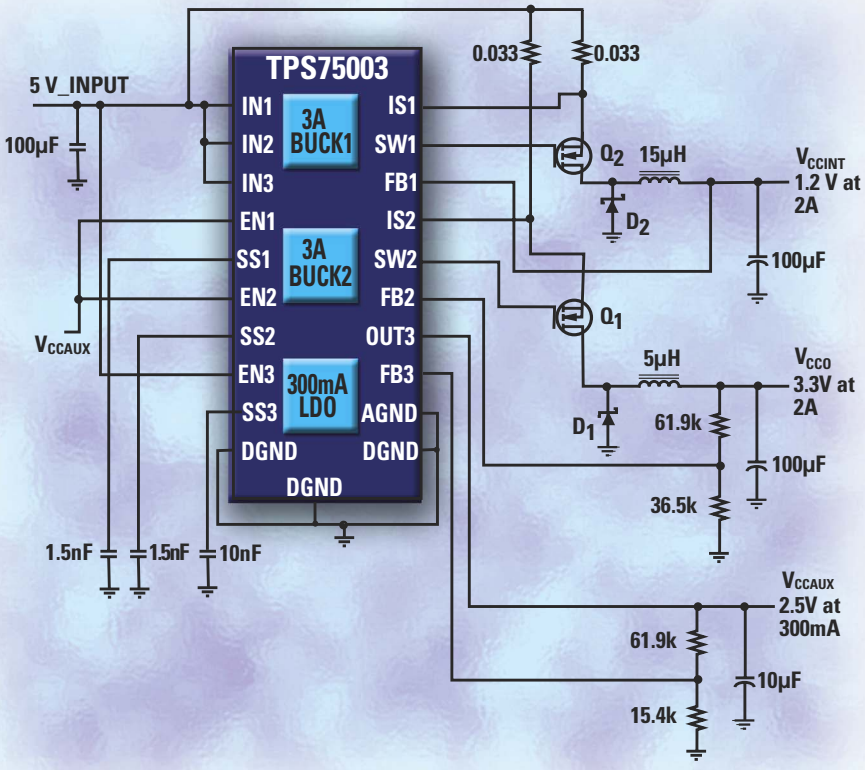
▶BivarOpto, www.bivar.com.



The LK Series of 60-lumen LEDs use a metal-core pc-board assembly to yield a 1W SMT design with integrated lens.

POWER MANAGEMENT

Triple Supply Powers Spartan™-3



▸Applications

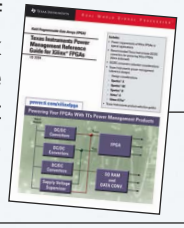
- DSL modems
- Set-top boxes
- Plasma TV display panels
- DVD players

▸Features

- Two 95%-efficient, 3-A buck controllers and one 300-mA LDO
- Adjustable output voltages
  - from 1.2 V for bucks
  - from 1.0 V for LDO
- Input voltage range of 2.2 V to 6.5 V
- Independent soft-start for all three power supplies
- LDO stable with small ceramic output capacitor
- Independent enable for each supply for flexible sequencing
- 4.5 mm x 3.5 mm x 0.9 mm 20-pin, QFN package
- $1.90: 1 K price

The **TPS75003** power management IC for Xilinx's Spartan™-II/IIE/3 series of FPGAs integrates multiple functions to significantly reduce the number of external components required and simplify design. Combining increased design flexibility with cost-effective voltage conversion, the IC includes programmable soft-start for in-rush current control and independent enables for sequencing the three channels. The TPS75003 meets all Xilinx startup profile requirements, including monotonic ramp and minimum ramp times.

For more information on TI's complete line of power management solutions for Xilinx FPGAs—including a library of reference designs, schematics and BOMs—visit **www.ti.com/xilinxfpga-u.**



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Tool analyzes ICs

Giga Scale Integration claims that its new IC-economic-analysis tool can help you figure out whether a foundry's less expensive, standard 90-nm process or even its 130-nm process will meet your design requirements just as well as the same foundry's pricier, low-power, 90-nm process. The technology expands on the company's InCyte chip-estimation tool, which allows users to derive an IC specification with estimates on die size, power, performance, and leakage. The company has now taken the estimation technology a step further by creating an economic analysis add-on engine to InCyte that allows users to turn their design specification into an IC budgetary quotation and figure out the best foundry and fabric for their next design project.

Adam Traidman, Giga Scale IC's president and chief executive officer, says that the company gathered silicon-wafer-pricing and defect-density data from foundries and trade groups, package-pricing data from packages, and test- and assembly-cost data from various vendors. The InCyte economic engine's database stores that data. "We take the output of our InCyte tool, which provides technical chip estimation for die size, power consumption, and number of pins, and combine that data with the new economic data to produce this final packaged-chip cost," says Traidman.

The engine also has a life-cycle-analysis feature that allows designers to forecast and account for mask re-spins, increasing yields, and decreasing wafer and package costs. Traidman says that Giga Scale will eventually improve the tool to allow users to analyze whether they should implement their designs in FPGAs, structured ASICs, or traditional cell-based-ASIC fabrics. The economic engine is available as a $2000 upgrade to InCyte. InCyte is available as a free download at www.chipestimate.com.

—by Michael Santarini

▷**Giga Scale Integration**, www.gigaic.com.

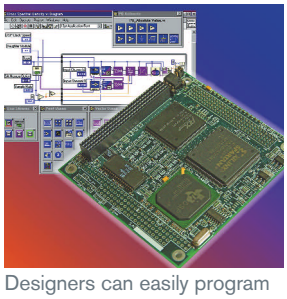
Embedded DSP simplifies programming

Sheldon Instruments' recently released SI-C6713DSP-PC104p embedded DSP board in the PC/104-Plus form factor targets real-time test, measurement, and digital-control applications. With a typical power consumption of only 2.25W, the board features the latest 300-MHz TMS320C6713 DSP from Texas Instruments and as much as 256 Mbytes of SDRAM. An expansion site for a family of multifunction I/O modules extends the DSP power with as many as 64 analog inputs and 16 analog outputs; a timing interface with two digital synthesizers and four counters; and a digital interface that comprises 32 bits of general-purpose I/O, two quadrature encoders, two frequency counters, and two PWM outputs.

The board comes with DSP-software libraries that enable system engineers to directly program their DSP systems in Visual Basic or National Instruments' (www.ni.com) LabView. However, for those who require custom development, the conventional C/C++-based tools have source-code-distribution support. Prices for the SI-C6713DSP-PC104p board with a 300-MHz DSP and 64 Mbytes of SDRAM start at $1985, and prices for I/O modules start at $595.

—by Warren Webb

▷**Sheldon Instruments**, www.sheldoninst.com.



Designers can easily program the SI-C6713DSP-PC104p board in LabView and Visual Basic. The board incorporates the TMS320C6713 DSP operating as fast as 300 MHz.

FEEDBACK LOOP

"Many (software engineers) are actually other types of engineers that became involved with programming in school or on the job through necessity. Often facing a time crunch, they write only enough code to make the project work, rarely giving any thought to quality code."

Joseph Travis, in *EDN*'s Feedback Loop on www.edn.com/article/CA601846. Add your comments.

07.07.05

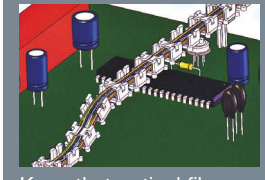
Physical guide routes optical guide

Even optical fibers, although relatively rugged, may still need some support and protection when designers cram them into today's tight and crowded boxes and systems. The OFFGS (optical-fiber-flexible-guide system) from Richco Inc provides the needed routing and channeling for 250- and 900-micron fibers. The flexible guide lets designers snake the fiber around the pc board and within the box and provides consistent placement and basic protection.

According to Cheryl Cummins, marketing manager at Richco, the OFFGS is available in a flat style for mounting directly to the pc board and with support posts that raise it above the pc board, so that it can go over ICs and other obstructions. A standard OFFGS piece measures 6.5 in. (16.5 cm) long and costs about $2.

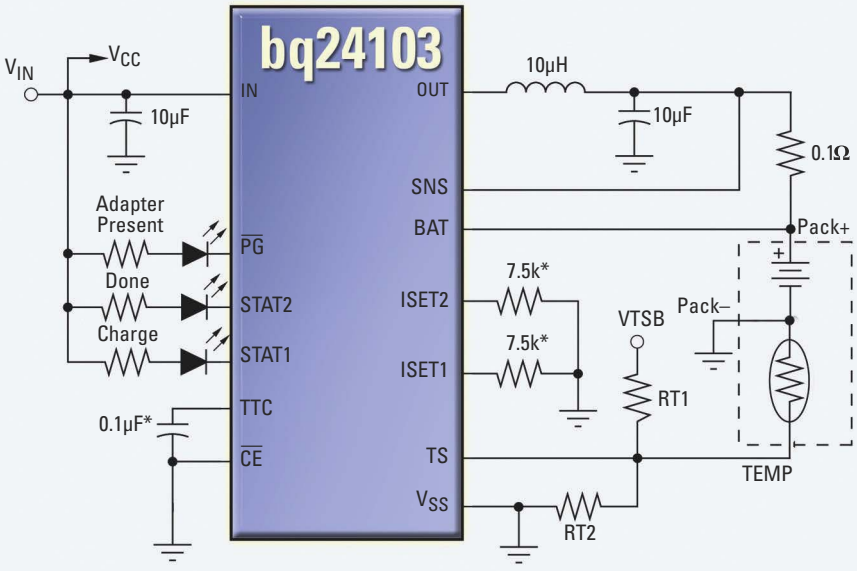
—by Bill Schweber

▶Richco Inc, www.richo-inc.com.



Keep that optical fiber well-behaved and constrained within your pc-board-based product with a flexible guide from Richco.

Integrated FET Switch-mode Charger



*I_{Charge} = 1.33A, $I_{Precharge}$ = 0.13A, Timer = 260 min

Synchronous, High-efficiency 2-A Switch-mode Lithium-Ion Charger Fits in 3.5 x 4.5 mm² QFN Package

The **bqSWITCHER**, the industry's first family of synchronous switch-mode battery charger ICs with integrated FETs, provides faster and cooler charging in portable applications. Ideal for high-efficiency charger designs with up to three Lithium-Ion battery cells in series, the bq241xx enables a small and simple solution by requiring only a few external components.

bqSWITCHER Products

Device	Charge Regulation Voltage	Application	Price*
bq24100	1- cell (4.2 V)	Standalone	$2.10
bq24103	1- or 2- cell selectable	Standalone	$2.20
bq24105	Externally programmable (2.1 to 15.5 V)	Standalone	$3.50
bq24113	1- or 2- cell selectable	System-controlled	$2.20
bq24115	Externally programmable (2.1 to 15.5 V)	System-controlled	$3.50

*Suggested resale price in U.S. dollars in quantities of 1,000.

▸ Applications

All 1-, 2- and 3-cell Li-Ion battery-powered applications:

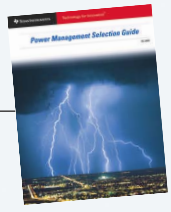
- **Portable DVD players**
- **Portable media players**
- **Handheld devices**
- **Industrial equipment**
- **Medical equipment**

▸ Features

- **Charges 1, 2 or 3 Li-Ion cells**
- **Synchronous 1.1-MHz PWM converter**
- **Highly integrated:**
  - **2-A charge FETs**
  - **Reverse-blocking diode**
  - **Thermal shutdown**
- **Battery management features maximize capacity, cycle life and safety:**
  - **Accurate voltage and current regulation**
  - **Charge conditioning, status and termination**
  - **Battery detection**
  - **Safety timer**
  - **Temperature monitoring**

▸ Packages

- **20-pin 3.5 x 4.5 mm² QFN**
- **Lead-free, RoHS-compatible**



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Emulators speed event-based verification

Tharas Systems Inc has released two new emulator systems that use multiprocessor SOCs (systems on chips). The single-user Hammer S-Class emulator has a capacity of 16 million gates and targets hardware designers needing to speed event-based verification. The multiuser Hammer M-Class emulator has a 64 million-gate capacity and targets hardware engineers who want to verify their designs, and, through the new Virtual Connect add-on, software engineers, wishing to get a jump on software development. Richard Curtin, senior vice president of marketing and business development for Tharas, says that the two new systems improve on the company's previous offering, the Hammer 100 system, on just about all fronts.

Whereas the Hammer 100 used 128 processors, had a 32 million-gate capacity, and ran an 8 million-gate design with a testbench operating at 4.5 kHz, the new S-Class uses 1024 custom processors, has twice as many gates, and runs the same 8 million-gate design at 50 kHz. The M-Class has 4096 processors, a fourfold gate increase, and the ability to run the same 8 million-gate design at 200 kHz.

Curtin attributes the speed and capacity improvements to the company's placing 32 of its Hammer 100 custom processors on one SOC. This approach increases the capacity and exponentially speeds the emulators and allows Tharas to offer the systems in a form factor the size of a big toaster. Tharas also custom-designed the instruction set to handle Boolean operations for simulation. Custom instruction-set simulation speeds emulation. The company has also worked extensively on the compiler to help users quickly load their designs onto the emulator systems. Curtin claims a 50 million- to 60 million-gate compilation time. The emulators accept Verilog- and VHDL-design files; assertions in OVL (object-verification language), OVA (Open Vera assertion), and PSL (property-specification language); and testbenches in Verilog, VHDL, or C/C++.

Tharas also offers a software add-on that allows embedded-system engineers to get a jump on software development. The company's Virtual Connect add-on has three flavors of software models targeting popular market segments: the Virtual-PC platform for graphics applications, the Virtual-Net for networking applications, and Virtual-3G for wireless applications.

Curtin says that most users are designing ASICs with 5 million to 6 million gates. "A 16 million-gate system, such as the S-Class, should cover most design groups for the next couple of design projects," he says, arguing that manufacturers will realize the value of the emulator for its increased speed versus simulation over the life of the system. Prices for the Hammer S-Class start at $200,000 for a 4 million-gate configuration, and prices for the M-Class start at $750,000 for a 32 million-gate configuration. Tharas also rents its emulators. Price of an S-Class rental in an 8 million-gate configuration starts at $21,000 per month. Price of an M-Class rental in a 32 million-gate configuration starts at $52,000 per month. Prices for the Virtual Connect add-on start at $75,000.

—by Michael Santarini

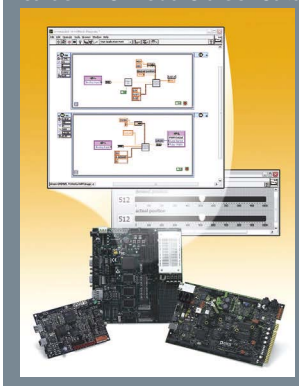
▷**Tharas Systems**, www.tharas.com.

Module enables graphical embedded programming

07.07.05

National Instruments recently announced an embedded-development module for its popular LabView software that extends graphical programming to any 32-bit embedded processor. With the module, designers can describe algorithms and program their applications using LabView's graphical data-flow language. In addition, LabView's graphical front-panel controls and indicators help engineers quickly and interactively experiment and debug their embedded code.

The LabView embedded-development module includes more than 400 analysis functions for signal processing, linear algebra, curve fitting, statistics, and calculus. The module also features a structure for integrating I/O drivers and board-support packages to take advantage of specific processors. Designers can develop their applications using the LabView graphical environment and then automatically generate C code to integrate with their chosen processor tool chains.



The new LabView embedded-development module provides designers with a graphical approach to custom embedded-system development.

James Truchard, PhD, chief executive officer and co-founder of National Instruments, says, "The evolution of LabView beyond the PC will open embedded-system design to an entirely new class of developer–a more mainstream population of scientists and engineers." Prices for the module start at $9995.—by Warren Webb

▶National Instruments, www.ni.com/embedded.

FEEDBACK LOOP

"I have this idea that I can apply engineering design to stock prices as though they were signals and make a living that way. Hey, if it works, my income won't be limited, and I can't be outsourced!"

Anonymous, in *EDN*'s Feedback Loop on www.edn.com/article/CA529820. Add your comments.

Intersil Battery Charger ICs

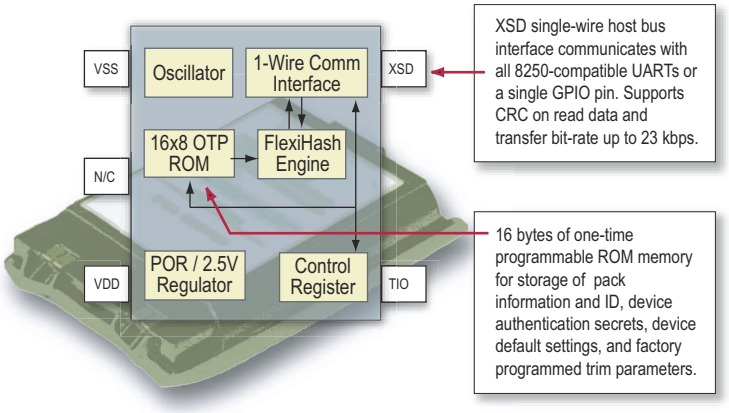
Intersil High Performance Analog

Don't Get Burned by Cheap Imposters

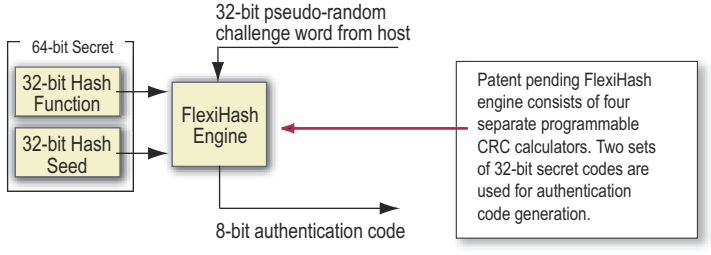
Protect your designs from counterfeit battery packs with Intersil's ISL6296. We've integrated our FlexiHash™ technology to deliver a simple, robust and inexpensive battery authentication solution for 1-cell Li-Ion/Li-Polymer or 3-cell NiMH series battery packs.

Intersil's ISL6296 offers the same level of effectiveness as other significantly more expensive, high maintenance, monetary-grade hash algorithm and authentication schemes. This device supports a wide range of operating voltages and is customized for low-cost applications.

ISL6296 Functional Block Diagram



Device Authentication Process



Key Features:

- Patent pending challenge-response authentication scheme using 32-bit challenge code word and 8-bit authentication code.
- Fast single-step authentication process
- Supports 1-cell Li-Ion/Li-Polymer and 3-cell series NiMH battery packs (2.6V-to-4.8V operation)
- Compatible for use with serial ports offered by all 8250-compatible UARTs or a single GPIO pin
- "Zero Power" sleep mode after bus inactivity time-out period
- 64-bit user-programmable secret for security
- Can also be used in a variety of accessories such as printer ink cartridges where authenticity needs to be verified.
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Q&A

Todd Westerhoff

EDA industry should use what it sells

As a high-speed-design manager for Cisco Systems Inc and a former product manager for Cadence Design Systems, Todd Westerhoff feels the pain of EDA customers he used to sell to and advise. He has 25 years of experience in modeling and analyzing electronics systems. Currently, he and his team of 10 focus on signal integrity and support other design groups at Cisco. Westerhoff earned a bachelor's degree in electrical engineering from the Stevens Institute of Technology (Hoboken, NJ). He vented his frustrations about EDA tools in an interview after a recent vendor panel sponsored by the EDA Consortium.

What do you do at Cisco?

A We use simulation tools to model the behavior of chips and the way we interconnect them at the board level. The limiting factor is that the speed of light is too slow. Circuits are switching so fast that the way a signal propagates is like a wave front. We can no longer consider circuits as lumped elements but rather as distributed structures like a wave.

Where does EDA come into the picture?

A In the past, you'd put these boards onto an oscilloscope or analyzer, but we use off-the-shelf simulation tools to increase the chance of first-pass success. The cost of mistakes in board design is prohibitive. The problems we face are so complex, you can't fix them simply by trial and error. We have to use simulation tools before we "fab" out the board.

Why do EDA tools fall short?

A The things we are trying to do, such as determine how an ASIC works with other chips, is a fantastically complex problem. It requires multiple tools to predict the board's behavior. Even the vendors that say, "We have a full solution" don't cover the myriad details associated with modeling and manufacturing the board. The problem of building something and bringing it into manufacturing has a million angles.

Why does this problem evoke so much emotion?

A I don't know if I'd [sound off strongly in a public forum] again. But sometimes you have to shake people up to get them to do things differently. I've been saying [EDA companies should use their products in actual design] for seven or eight years, and, obviously, not a lot of people are listening. We spend a lot of time and money on getting these tools to work correctly. I don't know anybody who says their relationship with the EDA industry is a walk in the park. But we'd be a lot better off if these tools were tested in a real-world situation.

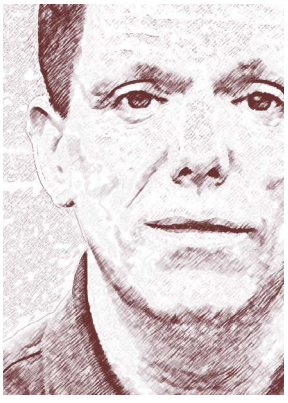
How did your transition from vendor to customer influence your thinking?

A When I got out of college, I spent 10 to 12 years as the guy marketing analog and digital simulators. Then I went out as a consultant using EDA tools, and it was a real eye opener. Instead of selling tools, I went to make a living using the tools. Many users never develop the comprehensive understanding of the tool that the vendors expect. User understanding of the tool is uneven, so everybody's perception of what needs improvement is different. The tool becomes difficult and complex to manage. They are big and complicated with many options. The user is saying "I just want to solve this problem." What grows out of that is you have tools that don't work or solve problems.

When I got into EDA around 1983, the paradigm was that, if you could get a computer to do what you wanted, you would be thankful. That [mindset] has never gone away with [EDA]. People tend to look at the problem from their own perspectives. It all changes when you turn around and try to use it, but if you don't use these things, you're not going to be able to perfect them. They're like race cars. You have to go to the track and beat them to death, or you're not going to win. It's also kind of like being in battle where everything is changing and going on around you. The last thing you need is to be in battle with tools that are unpredictable.

How do you cope?

A It's a constant problem and one we've learned to live with. The fascinating



thing is that some of the things we thought were trivial are big deals, and the things we thought were simple rough edges turn out to be big factors.

Please give an example.

A When I was a vendor, this schematic editor had all these fancy functions. Users came back and said that to put a component down and rotate it took seven mouse clicks, whereas our competitor's product required two. Vendors need to get things done repetitively right—not close, but right. You need to nail it. If it's something a user is going to do several hundred times a day, it is going to drive him crazy. And, if you're going to nail it, you've got to use it.

We can ask [a vendor] to add another bell or whistle to a simulator. [They say], "Here's this collection of capabilities. If we change it all around, maybe we can give them that feature." They might say, "We can't quite do this, but we can do something like it." That could be in 12 to18 months, and compromises get made along the way. In the meantime, the technology moves on.—by John Dodge

For an extended version of this interview, go to www.edn.com/050707/pq&a.

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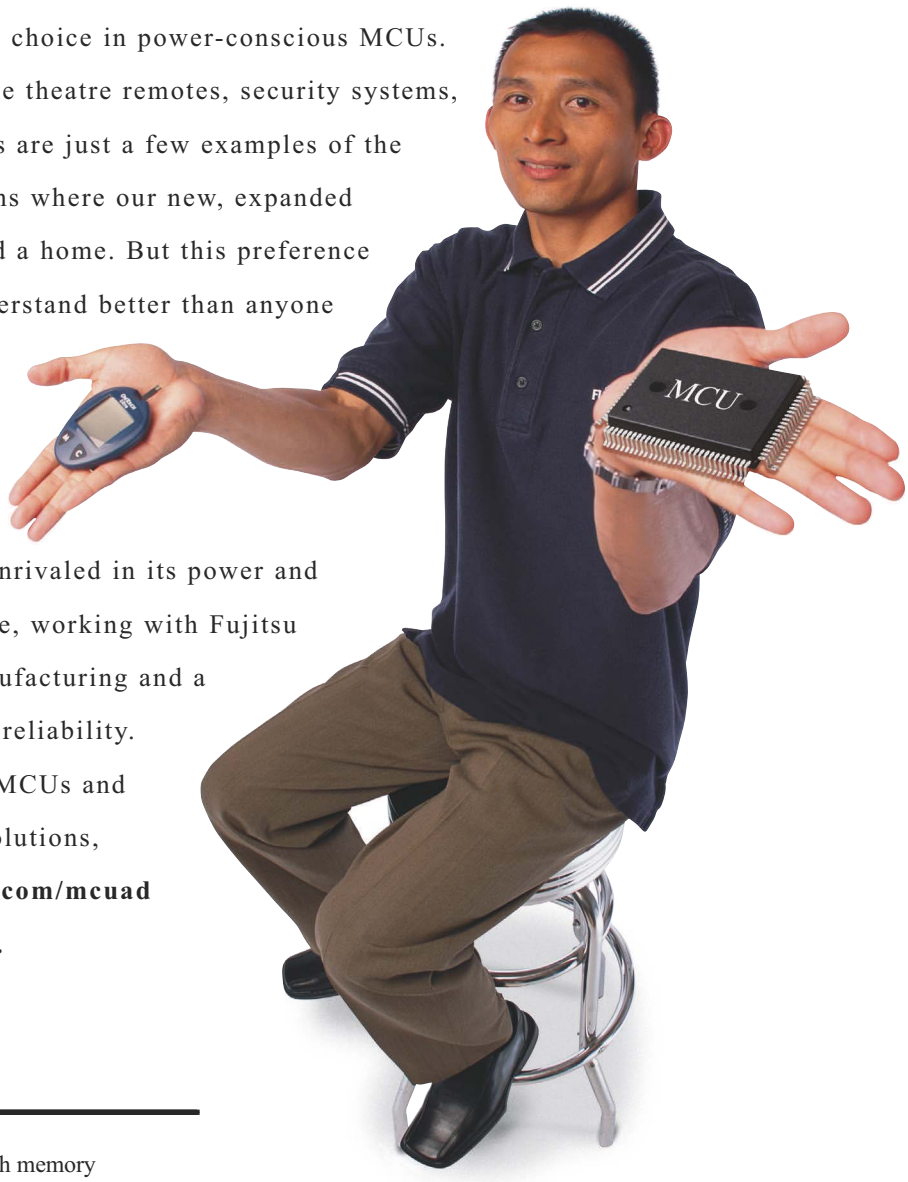

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WiCon panel opines on state of wireless standards

At the WiCon (Wireless Connectivity) World show in London in May, Mike McCamon, executive director of the UWB Forum (www.uwbforum.org), described as "an utter mess" the current situation of competing personal-wireless-connectivity standards. Partially giving rise to the description was the Bluetooth Special Interest Group's (www.bluetooth.com) May 2005 announcement that it intends to work with developers of UWB (ultrawideband) technology to "combine the strengths of both technologies." McCamon likens the proliferation of standards to the situation in wired networking around 1990. He looks toward a similar simplification in the same way that IP (Internet Protocol) came to dominate networking technology, anticipating that the wireless industry should be able to "clean up" the situation.

The UWB Forum stands on one side of the continuing UWB-standards wrangle, and the MBOA (Multiband OFDM Alliance) stands on the other. Nevertheless, Kursat Kimayacioglu, MBOA marketing-group member and director of wireless business development for the connectivity-business line at Philips (www.philips.com), echoes the sentiment. He looks to a more unified wireless environment in which the Bluetooth profile becomes just one of a number using the UWB-air interface.

The show provided a snapshot of progress toward functional UWB in its native mode; Freescale (www.freescale.com) operated a streaming-video demonstration with a claimed 100-Mbps link spanning 15 to 20m. This demonstration employed the first multichip implementation of its direct-sequence UWB silicon, and the company promises further integration. Visitors could also see file transfer over a wireless-USB link using first silicon of Staccato Communications' (www.staccato.communications.com) single-chip all-CMOS offering. Staccato envisages the technology's reaching the market on a time scale that would see external adapters for file transfer from PC to external hard drive early in 2006 and reaching high-end mobile-phone platforms in 2007.

—by Graham Prophet, *EDN Europe*

▷**Wireless Connectivity World**, www.wiconworld.com.

BITS & PIECES

▷**Yokogawa Electric Corp (www.yokogawa.com) of Japan has released the DL9000 series digital-oscilloscope platform for the 1-GHz band.** For more, see www.edn.com/050707p1.

▷**Wipro Technologies (www.wipro.com), the software services arm of India's Wipro Ltd, has created an SOC (system-on-chip)-based MP3 player that can operate either as a stand-alone chip or as part of a mobile phone.** For more, see www.edn.com/050707p2.

FPGAs implement high-end image-processing applications

New FPGAs with more DSP resources and embedded-processing capabilities have made the global image-processing market more competitive. According to Rahul V Shah, ASIC manager at eInfochips, an ASIC-design and -verification-services provider, designers can offload software-implemented algorithms, such as DCT, static Huffman, AES (Advanced Encryption Standard), color-space conversion, and gamma correction, to FPGA hardware. He claims that this approach improves system performance. Shah also notes that the conventional manner of implementing algorithms by software limits its performance due to serial data processing. Increasing frequency beyond certain limits causes system issues. FPGAs have flexible architectures and dedicated DSP blocks. Coupling these benefits with parallel processing strikes a proper balance in system performance and cost. FPGAs extend the flexibility to reprogrammability, resulting in a quick turnaround time.

According to Shah, parallel processing in hardware is impossible because hardware processing can execute instructions only one at a time. "If you want to run a DCT along with static Huffman with the same processor, one process at a time will execute," he says. "However, in hardware, because everything runs in parallel, you can have DCT and SHF [super-high-frequency] running in parallel at the same time without any performance hit." He adds that FPGAs provide the flexibility to upgrade to new standards and reprogram devices. For example, you can modify any system-level application to DDR and then move to DDR-2.

Designers can also reshuffle images to create applications, such as video cell phones, set-top boxes, LCD projectors, keyboards, videos, mice, and digital cameras and camcorders, among others. "Implementing DSP algorithms for image-processing blocks, such as DCT, AES, and static Huffman, requires a huge amount of memory, multiplier, and accumulator blocks," says Shah. For example, a DCT at 133 MHz can take as many as 64 multiplication and addition operations. Designers can map these multipliers onto the hardware to perform multiplication and addition operations, rather than do it sequentially in software. Static Huffman and AES cores have high memory requirements for storing coefficient values and performing mathematical operations on incoming data. Handling these operations in software slows down system performance and overloads the CPU. Offloading these tasks to the hardware means that the memory stores the image, and the CPU performs other control operations.

Implementing a dynamic Huffman algorithm in hardware would be a bad idea, because the algorithm requires dynamic calculations, which need a large amount of hardware, so proper partitioning between hardware and software is necessary. This approach is more cost-effective and provides better performance than running the algorithm in software.

—by Pradeep Chakraborty, *EDN Asia*

▶**eInfoChips**, www.einfochips.com.

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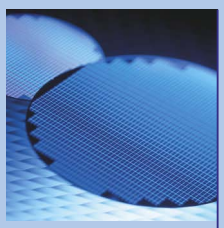

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Sensing Solutions: Part III

SENSING IN MISSION-CRITICAL APPLICATIONS

Part three of this three-part series on sensing solutions looks at high performance sensing systems, such as those used in ultrasound or MRI equipment. Susceptible to the slightest variations in power, noise, and signal latency, high performance sensing systems must deliver exceptional accuracy at extreme data rates — even a small error may be the difference between detecting cancer or not.

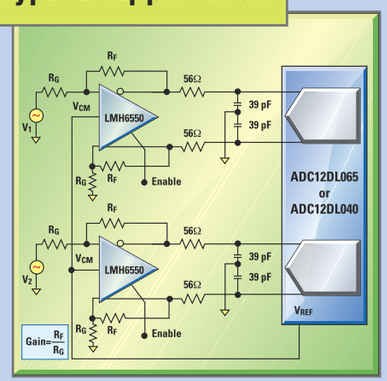
To read this case study, go to avnet.national.com

Delivering Exceptional Accuracy at Extreme Data Rates

This month, industry expert Nicholas Cravotta explores the unforgiving nature of working with high performance sensing systems in mission-critical applications, including:

- The importance of power supply stability and how to achieve it
- Managing high-speed sensor data flow through aggregation while minimizing signal skew
- Implementing effective signal conditioning to scale sampling voltage and attend to phase differences without compromising signal integrity
- Handling EMI and noise to maintain signal resolution and accuracy

Typical Application



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Wideband, Low Power, Linear-in-dB Variable Gain Amplifier

LMH6503
Wideband, Low Power, Linear Variable Gain Amplifier

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BY BONNIE BAKER

One in a million

Comparing devices from different manufacturers can be difficult not only at the bench, but also at the beginning of your investigation. If you start with the product data sheets, sometimes specification names don't match specification units of measure. In these cases, simple translations are useful in differentiating styles of units of measure.

You can glance at the far-right column of the specifications table within ADC data sheets and find the specification units of measure. The most common ADC dc units are least-significant bit (LSB), full-scale range (FSR), percentage of FSR, and number of bits (n). Some of the ac specification units are decibels for the signal-to-noise ratio (SNR) or the signal-to-noise-and-distortion (SINAD) ratio. These units of measure are standard parts of numerous converter data sheets, but the new, less-familiar parts-per-million (ppm) unit also appears in converter data sheets.

Note that the parts-per-million unit of measure usually appears in the 16-bit or higher resolution ADC data sheets. The fundamental questions you might ask are: What does this specification unit of measure mean to converter users, and why do the higher resolution converters usually have this unit of measure?

In data sheets for lower resolution converters, percentage of FSR appears as a unit of measure. Many converter manufacturers replace percentages with parts per million. This scenario is usually necessary if a percentage specification has too many zeros. For instance, say the gain error of a 12-bit ADC is ±2.5% of FSR. If you change this specification to parts per million, it becomes ±25,000 ppm of FSR. You make this change by moving the decimal point four places to the left. This example shows an impractical conversion because of the high number of zeros, which makes the specification difficult to read. In contrast, say the gain error of a 24-bit converter is ±0.005% of FSR. A more legible representation of this specification is ±50 ppm of FSR. When is one representation better than the other? The break-even point seems to be at less than 0.1% or at greater than 1000 ppm.

You can also use parts-per-million units to replace least-significant-bit units (**Figure 1**). A typical dc specification, such as integral nonlinearity for a 12-bit SAR converter, is ±1 LSB of FSR. If the FSR of this converter is 5V, the least-significant-bit size is 1.22 mV. 1 LSB equals the converter's FSR divided by number of bits, or FSR/2^{12}=1 LSB. The specification number becomes more cumbersome with higher resolution converters. As an example, a typical integral-nonlinearity specification for a 24-bit converter of ±15 ppm of FSR translates to an error of ±251 LSB of FSR. If the FSR of this converter is also 5V, the least-significant-bit size is 298 nV. To return to the original parts-per-million value, divide the least-significant-bit error by the converter's number of bits and multiply by 10^6.

The conversion from percentage or least-significant bit to parts per million is akin to the conversion from meters to inches, but the mathematics is more forgiving. Although this concept seems elementary, you would be surprised at how many engineers shy away from these representations on the units of measure. The fact that the units of measure in the right column seem to be unrelated from manufacturer to manufacturer discourages many people who compare competitive data sheets. But, in this situation, simple mathematics can put all of the products that you are evaluating onto the same playing field. EDN

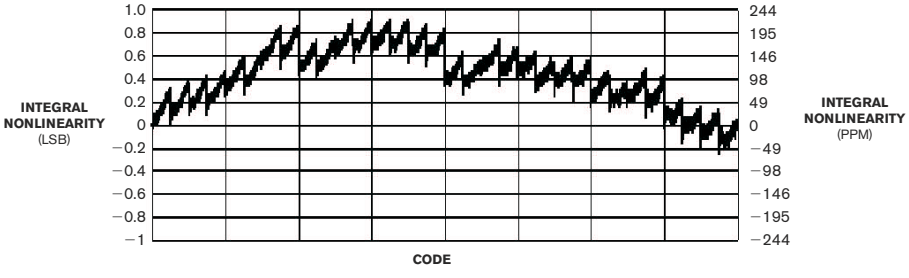

Figure 1 Converter-performance specifications can use either least-significant-bit or parts-per-million units. The two are mathematically equivalent but require that engineers pay attention to the conversion factor.

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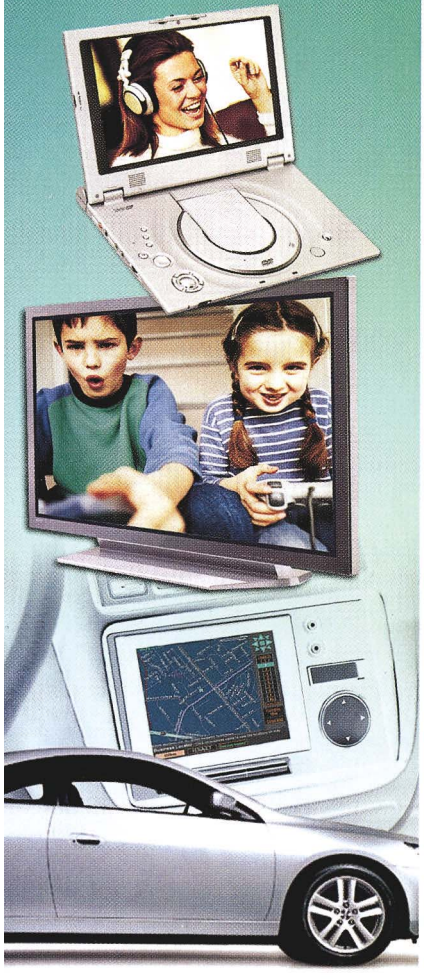
Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.baker@microchip.com.*

SIGNAL PATH designer℠

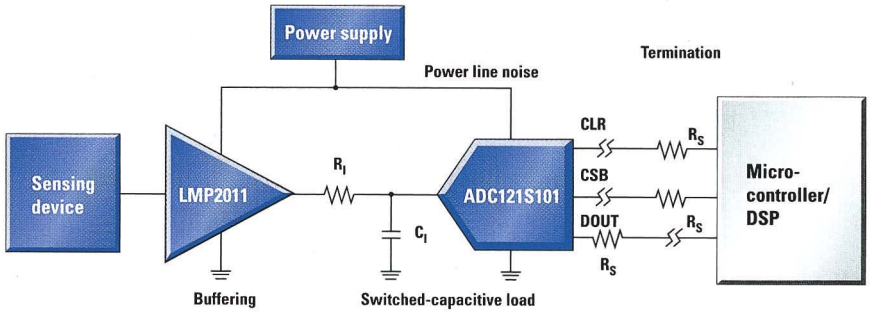
Tips, tricks, and techniques from the signal-path experts

No. 102



Maximizing Signal-Path Performance

— By Chuck Sins, Applications Engineer



Precision Signal Path

The signal path offers many opportunities for the system designer. In the analog-to-digital converter (ADC) signal path, making good design choices in buffering a sensing device, charging the switch-capacitive input of an ADC, and minimizing noise sources will maximize performance. All of these examples will be addressed in this issue of the *Signal Path Designer.*

Buffering a Sensing Device

When a sensing device is unable to drive the capacitive load of an ADC, it can be buffered with an operational amplifier (op amp). Since many applications require operation from a single supply, it is important to select an op amp that operates at the same voltage as the ADC. While sharing supply voltages helps reduce system complexity and cost, supply voltages place constraints on the input and output capability of the op amp. For ADCs such as the ADC121S101 where the reference voltage (V_{REF}) is both the supply voltage and the reference, op amps such as the LMP2011 with rail-to-rail output (RRO) capability are preferred. The LMP2011 with RRO capability allows the system designer to utilize the full dynamic range of the ADC, providing access to all of the output codes.

Once an op amp with suitable input/output capabilities has been selected, its gain bandwidth needs to be considered. For cases where the stimulus source's maximum output is less than V_{REF}, gain may be required from the buffering stage. The gain bandwidth product (GBWP) of an op amp specifies its

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High-Speed Signals, Clocks, and Data Capture

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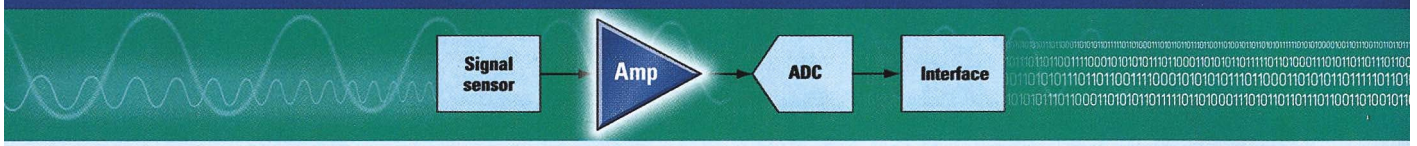
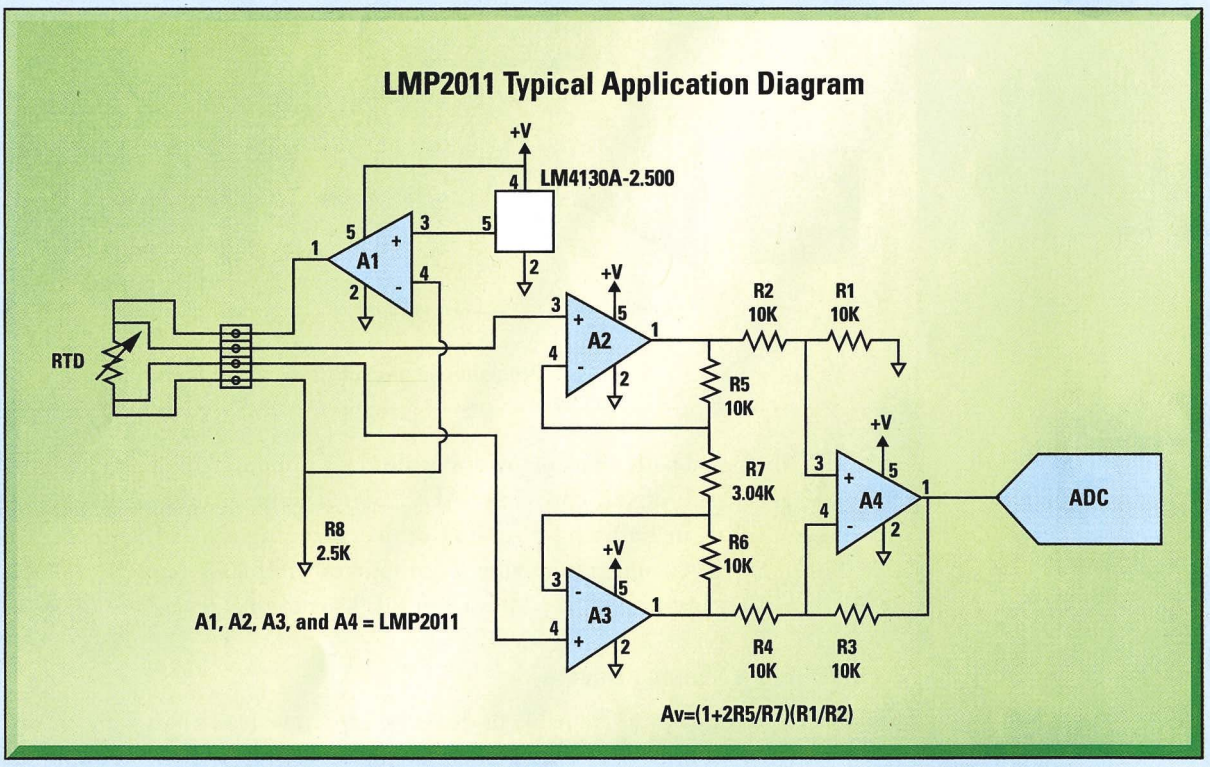
High Precision-Rail-to-Rail Output Amplifiers



Delivering High Precision Over Time and Temperature



LMP2011/12/14 Key Features → **System Benefits**

- 60 µV V_{OS} max over temp (- 40°C to +125°C) → Offers high accuracy measurements with continued accuracy over temperature
- Low voltage noise (35 nV/$\sqrt{Hz}$) and no 1/f → Increase signal accuracy during low frequency measurements
- High CMRR (130 dB), PSRR (120 dB) → High accuracy across voltages
- Gain (130 dB) and 3 MHz GBW product → Wide frequency range at higher gains

Maximizing Signal-Path Performance

bandwidth (-3 dB frequency) when configured as a unity gain amplifier. Since GBWP remains constant for a given op amp, a closed loop configuration with a gain of A_{CL} lowers the bandwidth by a factor of A_{CL}: $BW = \frac{GBWP}{A_{CL}}$

For example, the LMP2011 with a GBWP of 3 MHz will have a bandwidth of 300 kHz when configured with an A_{CL} of 10 V/V.

Because the closed-loop bandwidth is the -3 dB frequency of the amplifier, it is the frequency where the amplifier output is 70.7% of its input value. So at the –3 dB frequency there is a 29.3% error in output amplitude. Errors in ADCs are measured in units of least significant bits (LSBs). One LSB is defined as $V_{REF}/2^n$ where V_{REF} is the reference voltage and n is the ADC resolution. For example, 1 LSB of an 8-bit ADC is $V_{REF}/256$. For a system requiring $^1/_2$ LSB of accuracy from its ADC, the input stimulus must have gain accuracy of $(1-1/2^{n+1})$ or 99.8% for an 8-bit ADC. To guarantee that the op amp has sufficient gain accuracy for a given system requirement, it is necessary to calculate the maximum operating frequency (f_{max}) for the op amp. This is accomplished by approximating the frequency response of an op amp to be that of a single pole filter. The curve shown in ***Figure 1*** has the gain (A_V) and -3 dB frequency (f_o) normalized to 1.

The expression for this curve is

$$A_V = \frac{1}{\sqrt{1+(f)^2}}.$$

or solving for f,

$$f = \sqrt{\frac{1}{A_V^2} - 1}.$$

To achieve $^1/_2$ LSB of error from an 8-bit system, the normalized f_{max} of an op amp is

$$f = \sqrt{\frac{1}{(0.998)^2} - 1} = 0.062.$$

Therefore, for an 8-bit ADC with a $^1/_2$ LSB accuracy requirement, the op amp's effective bandwidth is 0.062 x GBWP. The LMP2011 with a GBWP of 3 MHz would have an effective bandwidth of 186 kHz when configured for unity gain. The effective bandwidth is further reduced if a gain greater than unity is required. The normalized f_{max} for

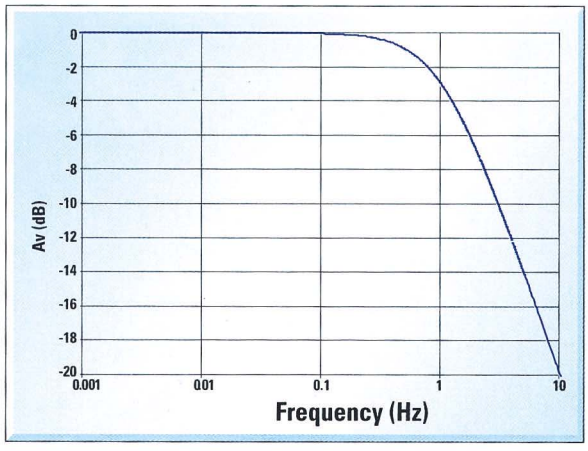


Figure 1. Op-Amp Frequency Response

$^1/_2$ LSB of error for ADCs of various resolutions can be calculated as:

$$\text{Normalized } f_{max} = \sqrt{\frac{1}{\left(1-\frac{1}{2^{n+1}}\right)^2} - 1}.$$

Transferring Charge to a Switched-Capacitive Load

The op amp was added to the ADC signal path to drive the capacitive load. However, the ADC's input is a switched-capacitive load *(see Figure 2)*.

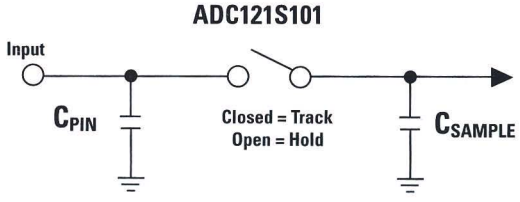
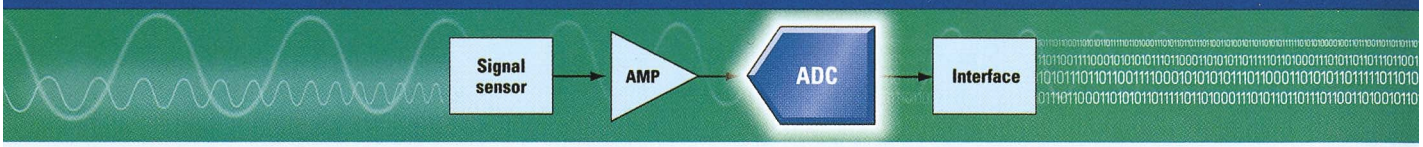


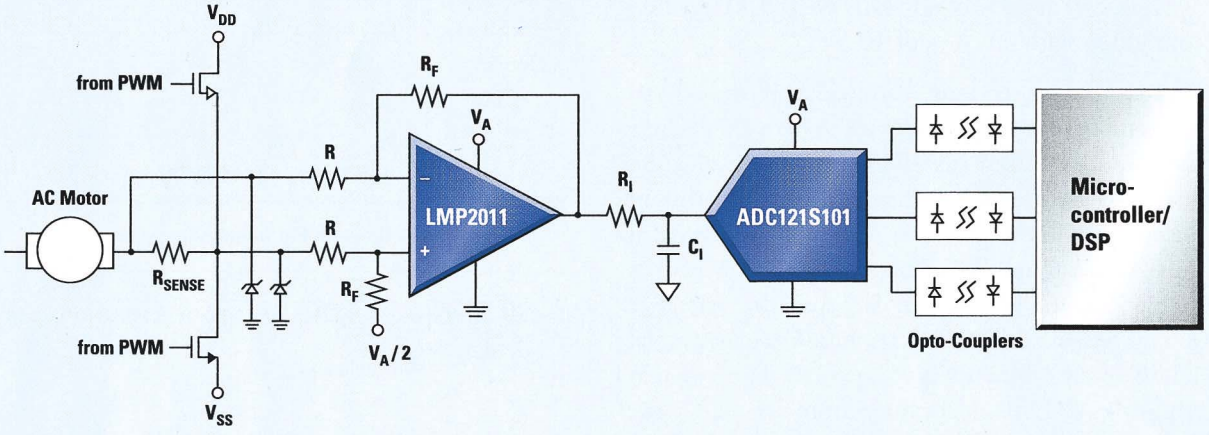
Figure 2. ADC121S101 Input

The ADC121S101 in "hold" mode has an input capacitance, C_{PIN}, of less than 4 pF, and in "track" mode has an input capacitance, C_{SAMPLE} plus C_{PIN}, of less than 30 pF. To minimize the error caused by the changing input capacitance, a capacitor (C_I) is connected from the input pin to ground. The C_I, which is much larger than the input capacitance of the ADC when in "track" mode, provides the current to quickly charge the ADC's sampling capacitor. An isolation resistor is generally added to isolate the additional load capacitance from the op-amp output *(see Figure 3)*.

Low power, high precision 8/10/12-bit, 1 MSPS ADCs



ADC121S101 Typical Application Diagram

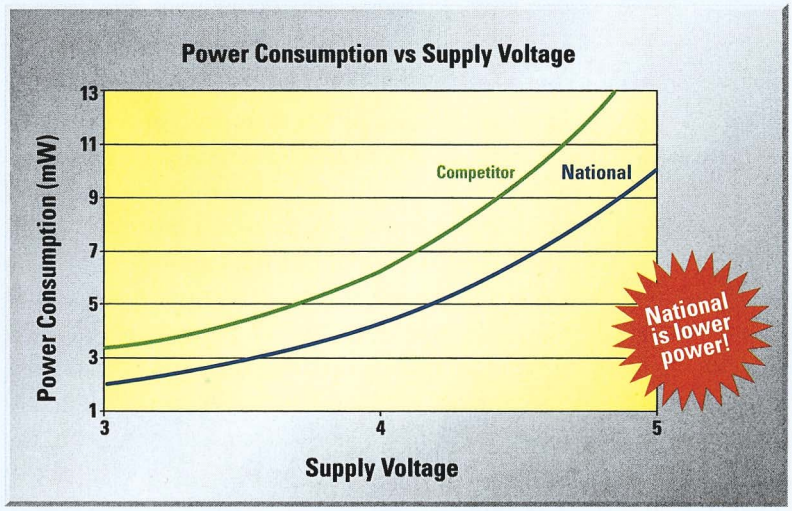


ADC121S101, ADC101S101, and ADC081S10 Features (typical)

- Speed range: 500 KSPS to 1 MSPS
- Integral non-linearity (INL): ±0.4 LSB
- Differential non-linearity (DNL): ±0.5 LSB
- Signal-to-noise ratio (SNR): 72.5 dB
- Signal-to-noise and distortion ratio (SINAD): 72 dB
- Spurious free dynamic range (SFDR): 82 dB
- Power consumption: 2 mW at 3V
- Supply voltage: 2.7 to 5.25V

Family Benefits

- Guaranteed performance over speed
- Pin and function compatible family
- Excellent static and dynamic performance
- Extremely low power
- Miniature packages reduce board space



Maximizing Signal-Path Performance

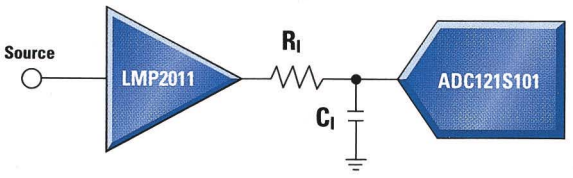


Figure 3. Quick-Charge Circuit

There are three important factors to consider in choosing appropriate values for the RC network. First, the designer needs to be aware that the RC network forms a low pass filter in the signal path. Therefore, the network can attenuate the sampled signal as the input frequency approaches the pole defined by $\frac{1}{2\pi RC}$. This is extremely critical for applications where ADC gain is important and no gain-calibration scheme is employed. Second, refrain from making the series resistor too large. While an increased resistance value decreases the phase delay at the output of the op amp (maintaining op-amp stability), it prevents the parallel combination of internal and external capacitance at the ADC input from fully charging during the ADC "track" time. Typical resistor values are less than 100 ohms. Third, make the external capacitor many times larger than the input capacitance while in "track" mode. Achieving this will minimize the drop in voltage on the capacitor when the ADC switches from "hold" to "track" mode.

The settling-time requirement of the op amp is determined by the amount of time the ADC spends in "track" mode. This is the amount of time that the op amp has to replenish the charge and reestablish the voltage on the capacitor prior to the ADC switching to "hold" mode. The time constant for recharging the capacitance at the input pin is defined by the series resistance value and the parallel combination of the internal and external capacitances. If the op amp fails to stabilize the voltage at the input by the time the ADC enters "hold" mode, inconsistent and erroneous conversions will result.

As a starting point for selecting values for R_I and C_I, the pole of the RC network may be set to the sampling frequency of the ADC. If this causes too much attenuation for the highest input frequency, the designer can decrease the capacitance or resistance values accordingly. The minimum resistor value should be set by the output drive capability of the op amp. Smaller resistor values are preferred since they limit distortion. However, the amplifier stability must be guaranteed over the full input frequency range, amplitude, and temperature of the application.

Managing Component Tolerance

If an inverting amplifier is used for the amplifier configuration *(see Figure 4)*, it is easy to calculate the error coefficient due to component tolerance. Since the gain is defined as $-R_F/R_G$, the maximum deviation from the ideal will occur when R_F is maximum and R_G is minimum or when R_F is minimum and R_F is maximum. If resistors with a tolerance of 1% are used, the maximum error will be 2%.

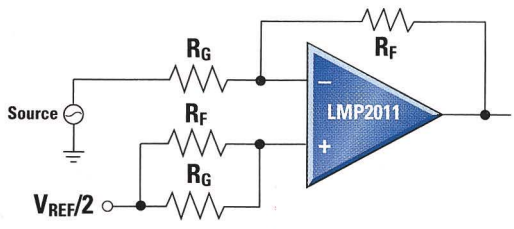


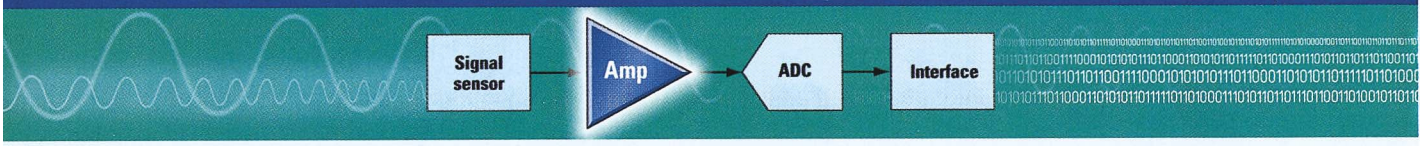
Figure 4. Inverting Amplifier Configuration

Applications where gain calibration schemes are not utilized must limit the dynamic range of the ADC. For an 8-bit ADC, 1 LSB represents 0.39% of V_{REF} (V_{REF} /2^n). Therefore, a 2% gain error due to resistor tolerance equates to a 12 LSB loss in dynamic range, 6 LSB (rounded up from 5.13) from the maximum output code and 6 LSB from the minimum.

Minimizing Power Line Noise

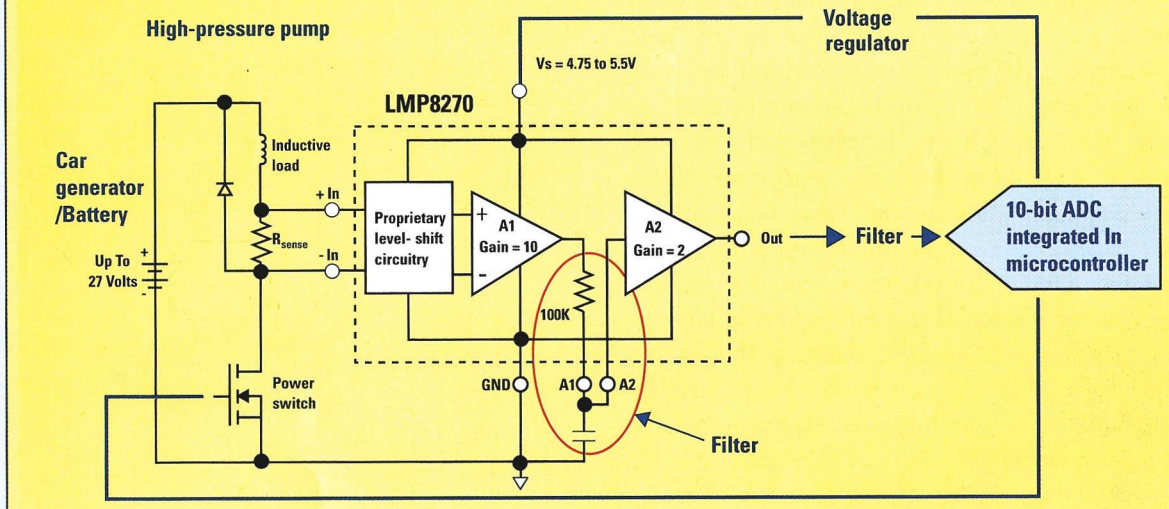
While component tolerance is one source of error in the ADC signal path, noise on power lines due to digital circuitry is another. Noise can couple into an ADC and an op amp through their supply pins. Typically, devices such as the LMP2011 have excellent power supply rejection ratios (PSRR) and will not be affected. However, ADCs such as the

High Common Mode, Voltage-Difference Amplifier



Precision Current Measurement in Automotive and Industrial Environments

LMP8270 Typical Application Diagram



LMP8270 Key Features

- Input offset voltage 1 mV max
- TCVos 15 µV/°C max
- CMRR 80 dB min
- Extended CMVR -2V to 36V
- Output voltage swing rail-to-rail
- Supply voltage 4.75V to 5.5V
- Temp range -40°C to 125°C
- Supply current 1 mA

System Benefits

- Initial system accuracy
- Continued accuracy over temperature
- Accurate under wide dynamic input currents
- Supports a wide range of input voltages
- Supports ADC input voltage levels
- Compatible with ADC voltage supplies
- Supports most automotive/industrial applications
- Minimum power consumption

Maximizing Signal-Path Performance

ADC121S101 whose supply voltage is also the V_{REF} have a PSRR value of 0 dB (no PSRR). The output drivers of the ADC itself have fast edge rates that cause the ADC to draw varying amounts of current. The noise introduced on the supply line can upset the ADC and other analog circuitry connected to it. A dual capacitor decoupling scheme with the smallest capacitor, typically 0.1 µF, placed within 1 cm of the supply pin and a 1.0 µF to 10 µF capacitor placed nearby is an excellent starting place for limiting supply noise. If analog and digital supply pins are connected to the same voltage source, a choke may be used between the pins. The choke will appear as a short at DC and a resistor at the higher frequencies where isolation is desired.

While good supply decoupling is always recommended, it is best to try and minimize the load capacitance seen by the output of the ADC so less current is required. Charging load capacitance causes noise spikes on the supply line while discharging load capacitance adds noise to the ADC substrate. There are several techniques to minimize load capacitance. The easiest way is to drive only a single device and place it as close as possible to the ADC output. It is also helpful to limit the effect of driving load capacitance by using series resistors, which limit the current required to charge or discharge the load capacitance and reduce the slew rate of the output. Limit the value of the series resistance to less than 100Ω to avoid violating the timing requirements of the digital circuitry. High-frequency systems may not tolerate the use of series resistors. Thus, it is essential that the driven circuitry be very close to the ADC output.

Maximizing Clock Integrity

Similar to ADC outputs, the ADC clock line can add noise to the system. The clock line should be treated as a transmission line when its length exceeds its rise time divided by 6 times the trace delay:

$$\text{line length} > \frac{t_{rise}}{6 \times t_{delay}}.$$

Trace delay is typically 150 ps per inch on an FR4 board. Treating a trace as a transmission line involves making the trace a controlled impedance with proper termination. This will help avoid signal reflection that can cause distortion. Distortion of the clock waveform leads to changes in the cycle-to-cycle clock period, better known as jitter. As the clock timing changes, there is variation in the exact point an ADC samples the waveform. With jitter, the ADC samples a point higher or lower on the signal than it ideally would. The net result of the time variation in the signal sampling point is noise. The maximum amount of jitter allowed for 1 LSB of error is $\frac{1}{2\pi f_{in}}$. For half an LSB of error, replace n with n+1.

Another technique for avoiding line reflection is line termination. There are two methods for terminating traces, near-end and far-end termination. Near-end termination requires a resistor in series with the line located close to the output of the signal source. The signal source resistance plus this series resistor should equal the characteristic impedance of the line. When near-end termination is insufficient, far-end termination is required. Far-end termination requires a resistor to ground at the clock input to the ADC. The terminating resistor is placed very close to the ADC input pin and the value should equal the characteristic impedance of the line.

When the clock source is required to drive multiple inputs, far-end termination alone may not be satisfactory. Far-end termination attenuates the signal level. Driving several inputs, each with a terminating resistor, may attenuate the clock voltage to the point that the logic thresholds are no longer met. For this instance, AC-termination is more appropriate. AC-termination requires a resistor in series with a capacitor to ground at the input to the ADC. This attenuates the AC component but not the DC component. For example, a signal that swings from 0 to 5V would remain centered around 2.5V in a system that is AC-terminated. The clock would still be attenuated but would be optimally centered between the CMOS trip points, allowing minimum signal swing to meet logic level-specifications.

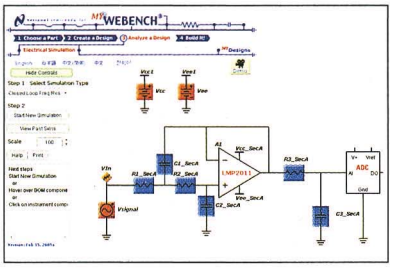
Summary

By making smart design choices in buffering a sensing device, charging the switch-capacitive input of an ADC, and minimizing noise sources, the performance of the analog signal path is maximized. ■

Design Tools

INTRODUCING...

Signal-Path Design Tool



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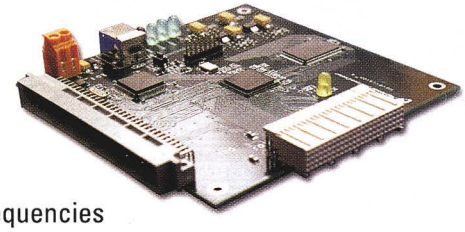

Features and benefits:

- Plug-n-play ADC evaluation board
- USB interface to PC
- PC-based data capture
- Easy data capture and evaluation
- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
- Produces and displays FFT plots
- Dynamic performance parameter readout with FFT
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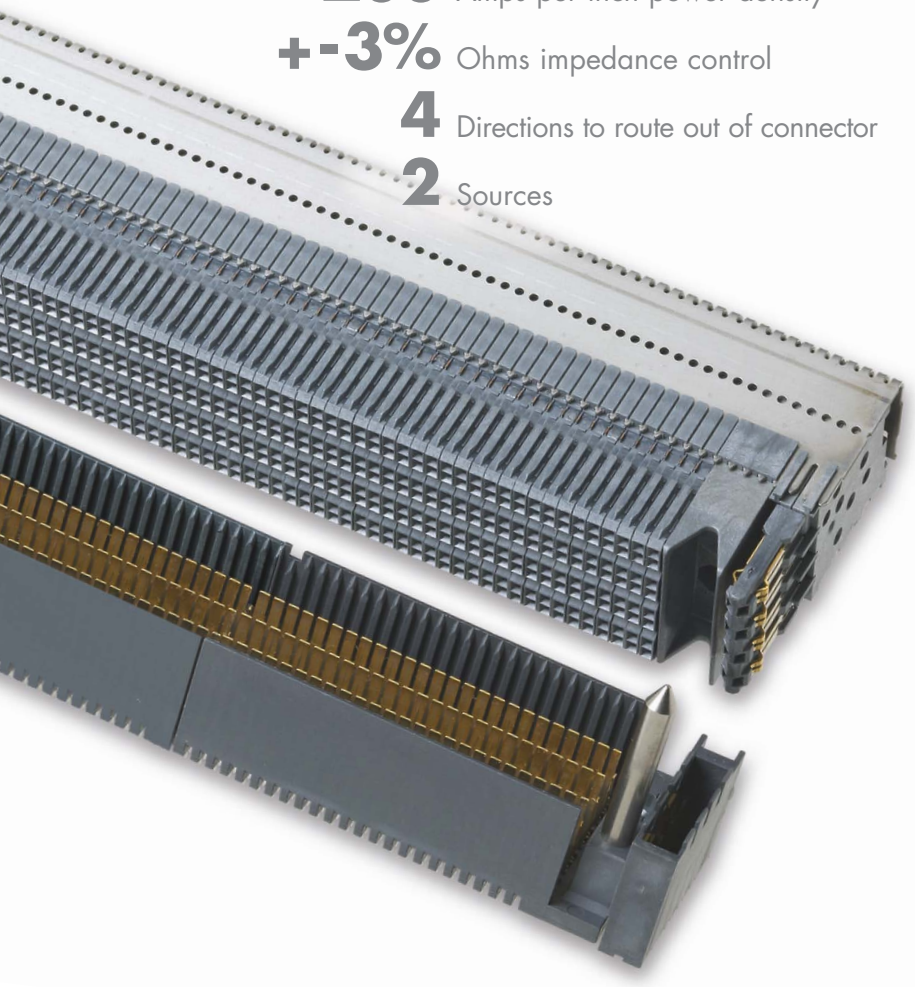
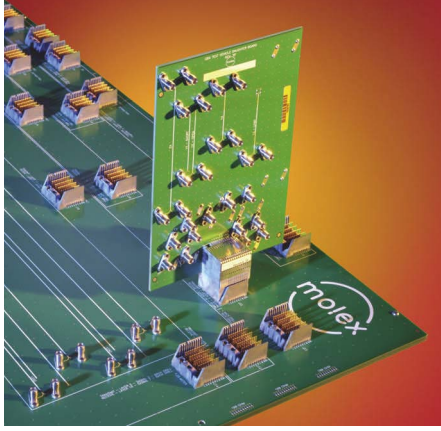
4 Directions to route out of connector

2 Sources





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Electronic passports embed contactless chip technology to streamline passage through customs and significantly hinder counterfeiters.

Contactless traveling

Much has been written over the past year about the transition to electronic passports. Reasonably minded privacy advocates attack potential security loopholes in the technology, and the lunatic fringe makes absurd claims about a grand governmental scheme to invade the privacy of the citizenry. In reality, electronic passports will ease the lives of travelers passing through customs, stymie counterfeiters, and provide governments with no more information than they currently gather from travelers. Even before the recent addition of Basic Access Control technology to the plan, electronic passports could not, as some have claimed, have allowed terrorists to wirelessly scan crowds or cafés for targets from specific nations. Still, the additional security measure will make a good thing better. When we focus our Prying Eyes, it's not about privacy; it's about how the electronic passport works.

An inlay based on flex-circuit technology is embedded in the rear cover of electronic passports. Axalto is one of the companies that has manufactured initial production samples for the US government to evaluate. Although manufacturing schemes will vary country by country, the US government will require a supplier to fabricate the passport cover with the inlay, and then the government printing office will add the pages, including the inside of the rear cover, with the standard printed ID information. The inlay must handle harsh environments, as travelers will surely bend, and even sit on, the books.

"Contactless chip technology" is the heart of the electronic passport. Vendors of inlays and ICs are careful not to use the term "RFID," but in fact, the electronic passport does use a secure form of RFID. An antenna coil runs around the perimeter of the electronic-passport inlay. An RF field stimulates the coil and activates the chip mounted on the flex circuit. The International Civil Aviation Organization (www.icao.org) developed the specification for the design. A reader must be within 4 in. of the specified circuit to power the chip and begin communications.

The chip at the base of the electronic passport is essentially a smart-card chip—a microcontroller that comes with encryption capabilities and a contactless radio interface that meets the ISO 14443 standard. Axalto has supplied the US government with coil-on-module inlays based on Infineon and Philips chips. North American-based Atmel targets the electronic-passport market with its AT90SC family. The AT90SC12872-RCFT, for instance, integrates an AVR RISC core, 72 kbytes of EPROM, 128 kbytes of ROM, a crypto-accelerator engine, and the radio interface.

The electronic passport requires authentication by a reader and uses encrypted communications with the reader for maximum security. Moreover, the scheme requires that the passport be open for communications to occur. Just as on existing passports, the new electronic version will include a printed ID page and, at the bottom of that page, some machine-readable codes. In that code, an optical sensor in the reader will find a seed for the two security keys needed for communication. The reader must compute the keys and use the first as an authentication key to wake the smart-card chip and use the second as an encryption key. A mathematically generated digital signature ensures that no one has altered any of the stored data.

Memory in the smart-card chip will store all of the ID data that appears on the printed ID page. From the biometric perspective, the United States will require that the memory store a digital representation of the ID photo. Other regions may add additional biometric data. The European Union, for instance, will store fingerprints in the memory.

Additional security measures may prevent electronic passports from rolling out on schedule, and unless the government issues a waiver delaying the process, visitors to the United States who have never needed a visa, will.

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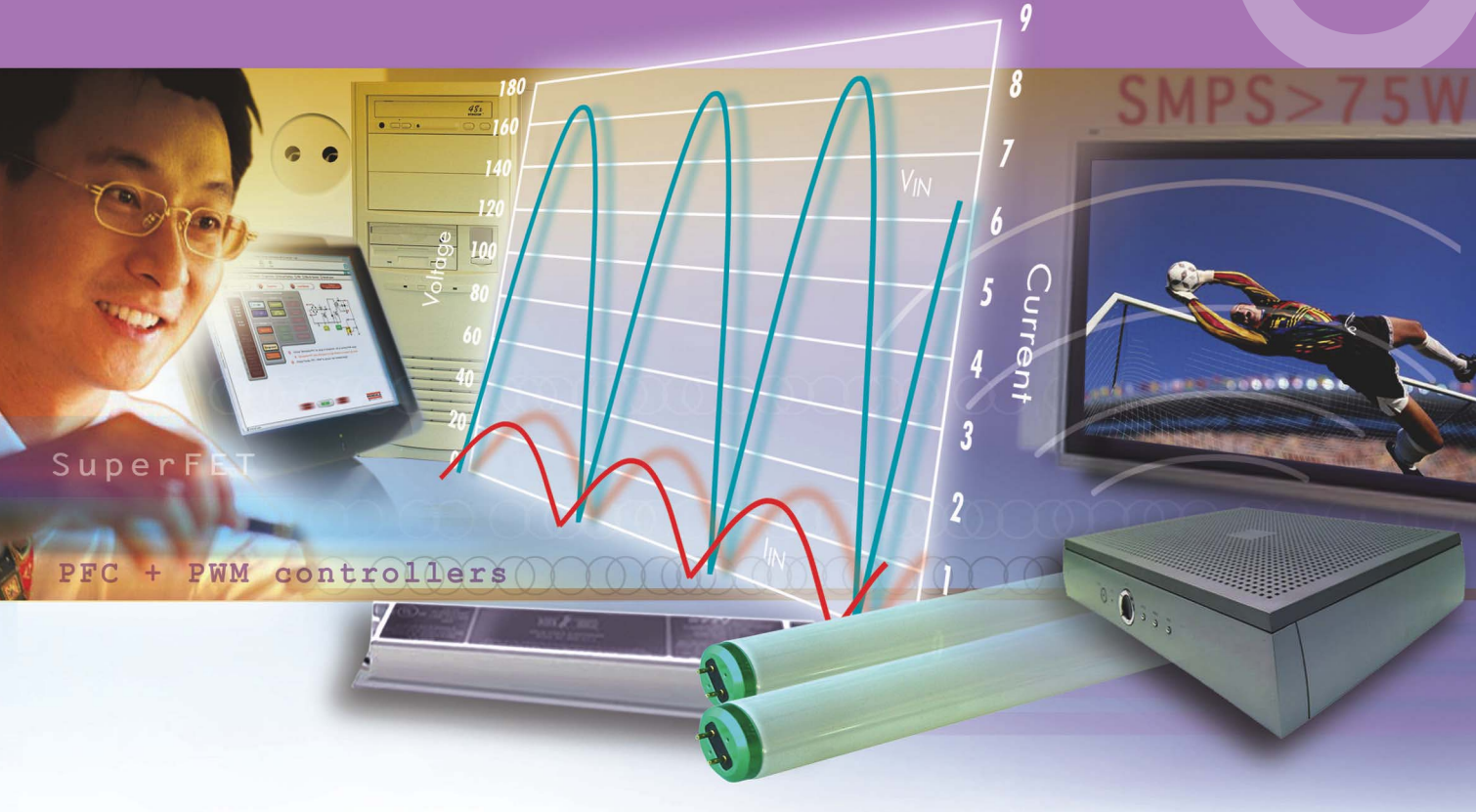

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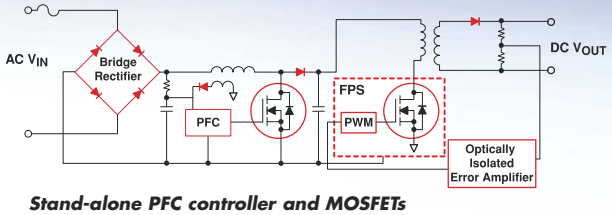
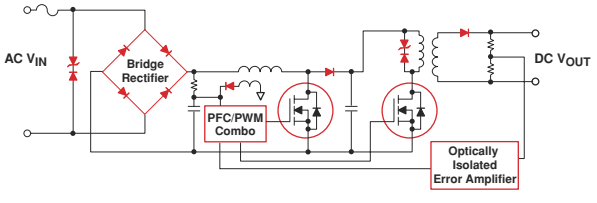


Stand-alone PFC controller and MOSFETs



Integrated PFC/PWM controllers and MOSFETs

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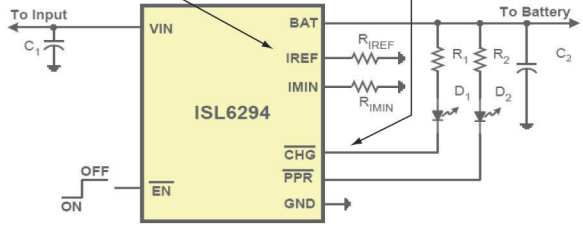
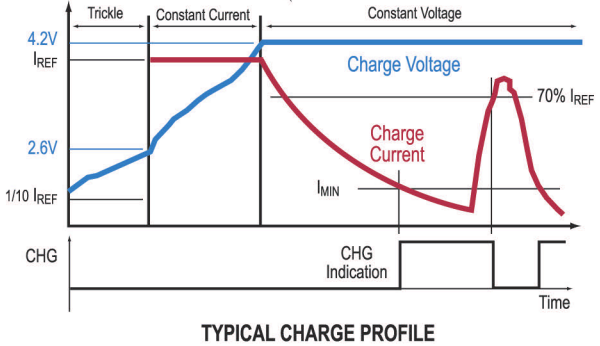
The constant current I_{REF} is set with the external resistor R_{IREF}. The constant voltage is fixed at 4.2V.

End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



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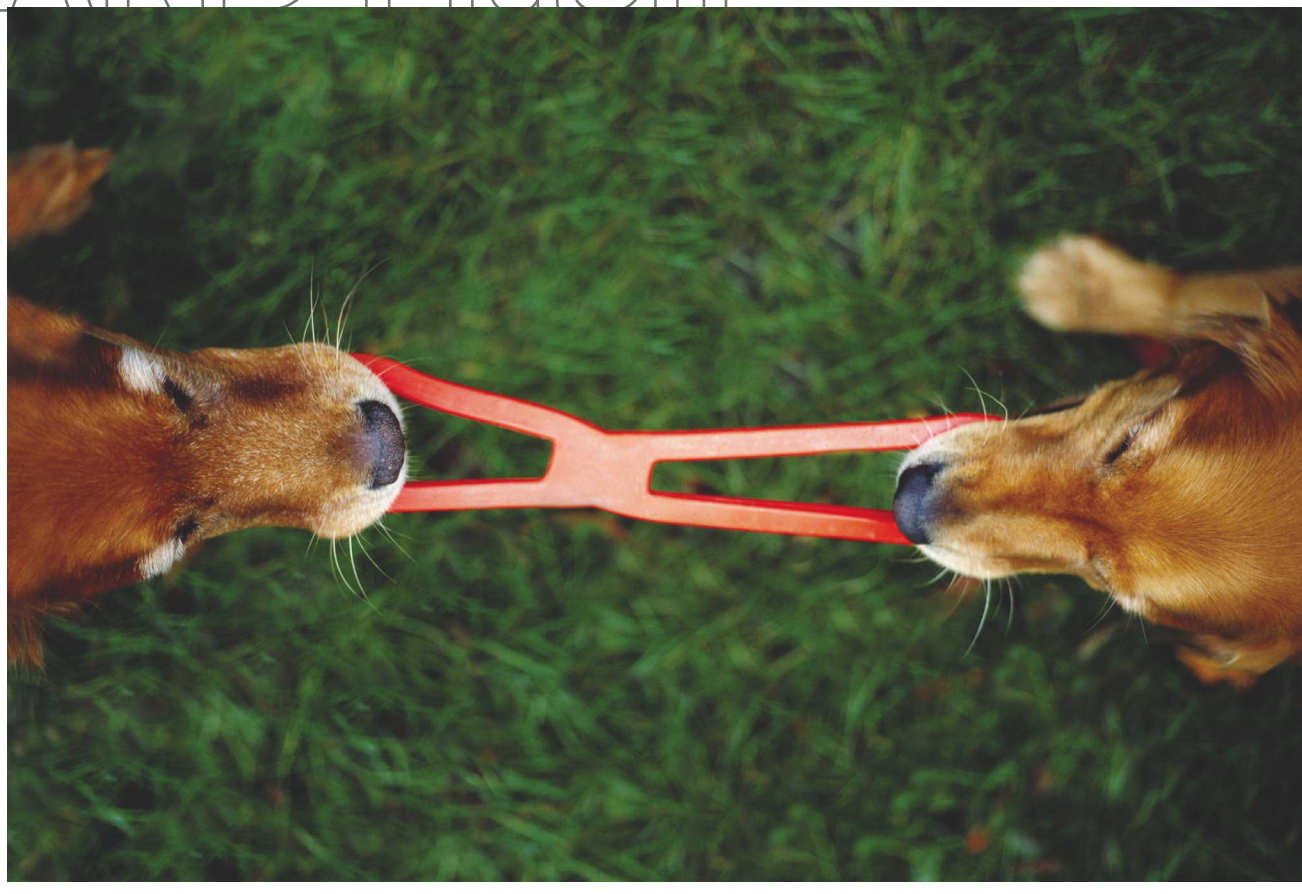

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CAT5 tracks: Audio goes the distance, reliably and on time

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

The next time you're at a music concert, take a look at the cabling that connects on-stage gear to the mixing board in the middle of the audience. Odds are good that you'll see one or several thick "snakes" containing bundles of wire, with each wire carrying a unique analog signal to or from the stage. Heavy? Bulky? EMI-radiating? Sensitive to environmental noise? You bet. All of these issues, and more, hamper the traditional analog-interconnect scheme. So, why is this seemingly archaic approach, mimicked in many recording studios and other audio-equipped environments (including churches, offices, and school auditoriums) still in use?

The wheels of progress in the commercial-, industrial-, and professional-audio industries move at a snail's pace. Gear is designed for long life in spite of rough handling, new-gear budgets are slim to nonexistent, and replacement and upgrade opportunities are consequently few and far between. And when these opportunities do occur, potential customers face a bewildering assortment of often-incompatible approaches, as vendors attempt to lock them into sole-sourced equipment suites. Still, the analog-to-digital conversion is under way, and de facto standardization driven by market leadership and attrition, aided by industry-standards bodies, is whittling down the diversity of options (see Brian's blog entry "Audio over CAT5: Proprietary alternatives and standardization efforts" at www.edn.com/briansbrain).

The "diversity-of-options" claim may baffle those of you who listen to streaming audio from the Internet or who route your server-housed music libraries to various pieces of LAN-connected gear in your homes and offices. Isn't conventional, commodity, and cheap TCP/IP-based Ethernet over CAT5 (Category 5) cable specified to a guaranteed 100m drive distance or, even better yet, no-cables-required WiFi (Wireless Fidelity)? (See **sidebar** "Cabling choices.") In some

AT A GLANCE

- Audio-tuned CAT5 (Category 5)-cable configurations travel into applications where TCP/IP fears to tread.
- CobraNet touts its compatibility with conventional Ethernet traffic, along with the backing of a major semiconductor supplier.
- MaGIC (media-accelerated global-information carrier) is slow out of the starting gate; manufacturers are folding some of its ideas into industry-standard committee activities.
- EtherSound delivers tight tolerances and minuscule latencies at the expense of Ethernet compatibility.
- AudioRail chooses a cost-optimized path that differs from its competitors' trails.

cases—more and more as technology progresses—it is. But in demanding audio environments, its time-insensitive, bulk-file-transfer heritage hinders its applicability.

Press "play" on your LAN- or WAN-connected audio receiver, and there's a several-second delay as the local buffer memory fills up. The buffer is there to compensate for protocol overhead and the inevitable packet-routing delays to come, resulting in out-of-order packet reception, along with the even more egregious network congestion, collisions, and other factors that result in packet loss and force retransmission or error concealment. Most home networks are, at any given time, lightly loaded—a situation that's quickly changing in the era of viceo streaming. However, you can't make the same assumption of commercial, industrial, and professional networks, particularly those handling multiple channels' worth of high-resolution audio, along with control *and* general data traffic (see Brian's blog entry "Audio over CAT5: Conventional counterparts" at www.edn.com/briansbrain).

Detectable latency is intolerable in a live-performance setting, and it's also unacceptable in most recording environments. What's "detectable"? According to Gibson's chairman and chief executive officer, Henry Juszkiewicz, whereas "university guys" might claim that the human eyes, ears, muscle, and brain can combine forces and detect picosecond-level latency, audio technologists should shoot for a half-millisecond latency through any network "hop." Professional musicians might be able to detect a total latency (that also encompasses analog-to-digital and digital-to-analog conversions, analog- and digital-audio processing algorithms, and other delays) on the order of 2 msec, but anything less than 5 msec is difficult for the average listener to perceive (see Brian's Blog entry "Audio over CAT5: Divide and conquer" at www.edn.com/briansbrain).

COBRANET STRIKES

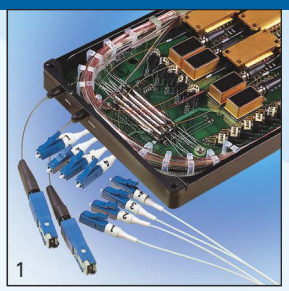
Although conventional TCP/IP-based CAT5 cabling may not currently address demanding audio-application needs, the volume-driven low cost of CAT5 hardware *is* attractive to hardware and software suppliers. Cirrus Logic's CobraNet technology, the fruit of the company's mid-2001 acquisition of Peak Audio, is one of the more mature contenders for the CAT5-audio throne and a market-share leader. CobraNet is also notable for its ability to coexist with other Ethernet traffic on a common set of network resources (**Figure 1**). However, its capabilities aren't *completely* unbounded; Michael Johas Teener—currently a networking architect at Broadcom and formerly the chief architect of FireWire at Apple—observes that CobraNet employs a "limited-topology" concept to ensure its claimed capabilities are achievable. "One extra switch, or a legal but 'non-CobraNet' configuration," his analysis states, and quality will be poor (see **sidebar** "Additional protocols," and **Reference 1**).

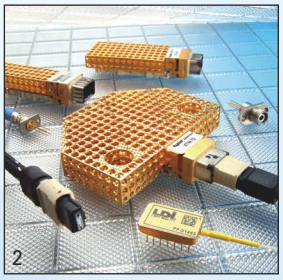
CobraNet's protocol combines one or more audio channels into an Ethernet packet, along with identifying data, such as the sample size and rate. It also enables you to send control information by bridging RS-232 data over Ethernet or generic Ethernet packets containing user-defined control data. The first-generation CobraNet transceiver modules contained digital logic housed in FPGAs alongside Motorola (now Freescale) DSPs and analog circuitry. Second-generation modules combine analog and digital circuits within a single CS1810xx ASIC , alongside a Cirrus Logic DSP. (Variants with 2×2, 8×8, and 16×16 channels are available.) Cirrus also launched DSP-inclusive CS4961xx product variants at January's Consumer Electronics Show. A multidimensional matrix of sample size, sample rate, number of audio channels to support, and desired latency—5.33, 2.66, and 1.33 msec—defines which chip variant your application will require. (See Brian's blog entry "Audio over CAT5: interesting lit and other bits" at www.edn.com/briansbrain for a downloadable spreadsheet from Cirrus Logic that will allow you to make the necessary calculations.)

CobraNet supports 48- and 96-kHz sample rates but, oddly, not the 44.1-kHz standard that Red Book Audio CDs and common audio peripherals employ. It also tackles samples as large as 32 bits. One showcase CobraNet installation, according to Senior Marketing Manager David Parker, is Tokyo Disney Park, which combines a gigabit Ethernet optical-fiber backbone and 250 nodes' worth of 100-Mbit Ethernet transceivers. This unified network handles data traffic related to lighting, ride controls, and point-of-sale cash registers, as well as distributed- and live-audio broadcasts. "The park is open seven days per week, 365 days per year," says Parker, "and any network failure would result in a complete park evacuation."

MAGIC TUNES UP

Back when Gibson was contemplating a move to a digital-guitar-to-amplifier-and-mixer interface, CobraNet still required upfront and per-channel royalty payments. And, pragmatically, the decision-makers at the company probably had visions of incoming royalty-revenue streams dancing in *their* heads, as well. So, Gibson went its own way, and MaGIC (media-accelerated global information carrier) was the result. (Zipi, a token-ring-based approach from the company, predates MaGIC.) Along with a FAQ, a full specification, and other materials, Gibson's Web site offers an approximately 10-minute video in Windows Media format that, among other things, outlines Gibson's sweeping vision for MaGIC as a control, multimedia, and general data-transfer protocol for the home. However, Gibson produced the video in 2001; since then, other companies and industry-stan-





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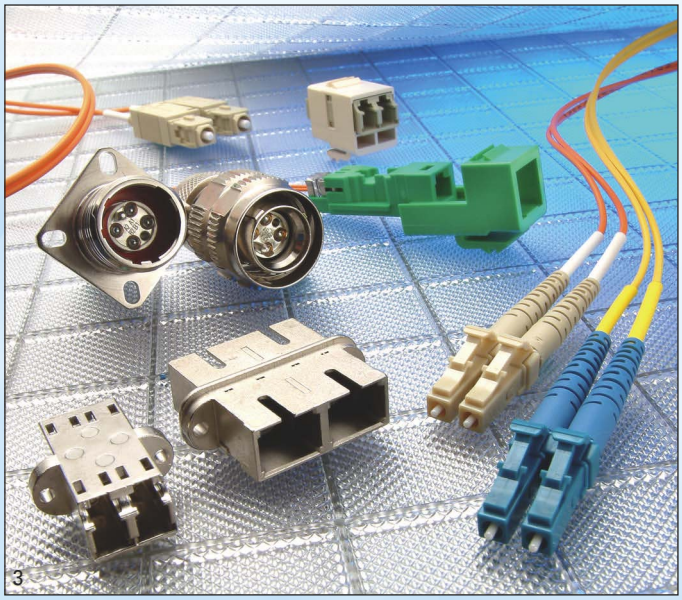

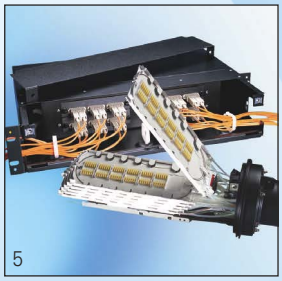

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dards bodies have produced alternative, now-dominant schemes for the consumer-electronics market, including Apple's Bonjour, UPnP (Universal Plug and Play), and Microsoft's PlaysForSure and Windows Media Extenders.

Nonetheless, Gibson still believes its approach has merit in commercial-, industrial-, and professional-audio settings. MaGIC provides as many as 32 channels of 32-bit bidirectional audio over 100-Mbit Ethernet with sample rates as high as 192 kHz. (As the number of channels increases, the allowable sample rate decreases, and visa versa.) Gibson claims that data and control transport occurs 30 to 30,000 times faster than MIDI (musical-instrument digital interface). Additional cable features include phantom power, automatic clocking, and network synchronization. And, notably, the MaGIC specification touts 250-µsec point-to-point latency times across 100m CAT5 spans.

These impressive performance specifications, however, come at the price of less-than-full Ethernet compatibility. MaGIC *does* conform to the IEEE 802.3 PHY (physical) layer and uses standard CAT5 cable and RJ45 connectors. (Ruggedized EtherCon connectors from Neutrik are also available.) However, it employs unconventional packet sizes and requires a unique MAC (media-access-control) implementation. The FAQ on Gibson's Web site states, "The footprint of our packet is the same as Ethernet UDP [User Datagram Protocol]. We differ from standard Ethernet because our packet size and transmission rate do not change ...We route on the MAC layer, which is Layer 2. We refer to data as frames on this layer instead of packets. Some parts of the MAC layer can be incorporated into software" (**Reference 2**).

Gibson is offering 10-year royalty-free MaGIC licenses to all interested parties, hoping to stimulate interest in the protocol as an industry-standard interconnect scheme. A $2500 software-development kit and a $600 evaluation board are available, as are VHDL implementations of the CobraNet transceiver targeting Altera and Xilinx FPGAs. Juszkiewicz acknowledges that a modern ASIC implementation will be necessary to hit cost targets in high-volume applications and is negotiating for MaGIC protocol support in future CobraNet silicon spins that target Gigabit Ethernet transfer rates. (Cirrus Logic has no comment on Juskiewicz's claims.) And where's the Gibson digital guitar that was supposed to be in production by the end of 2002? (See Brian's blog entry "Audio over CAT5: Hands-on jams" at www.edn.com/brians brain). Prototypes have existed for several

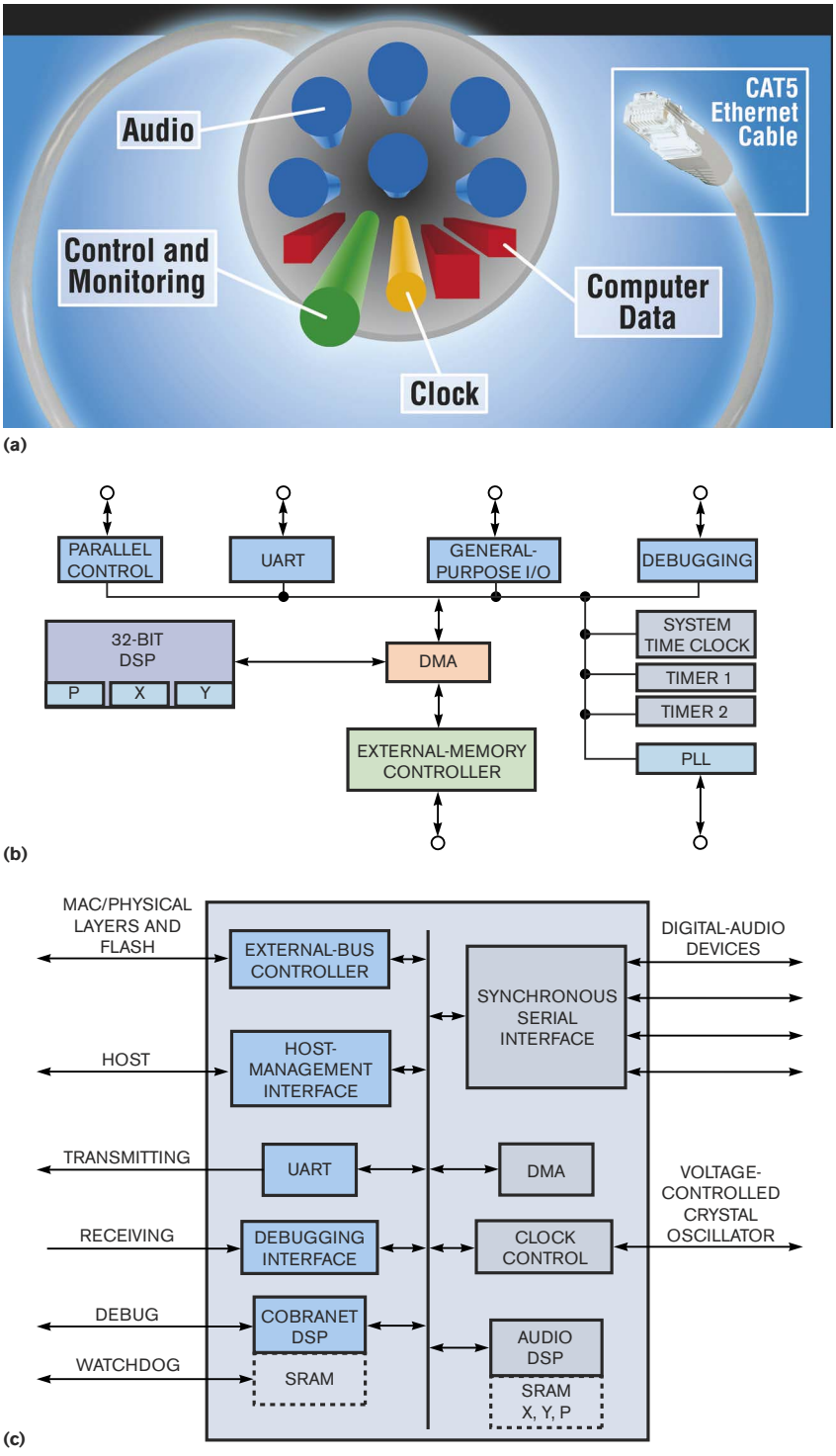
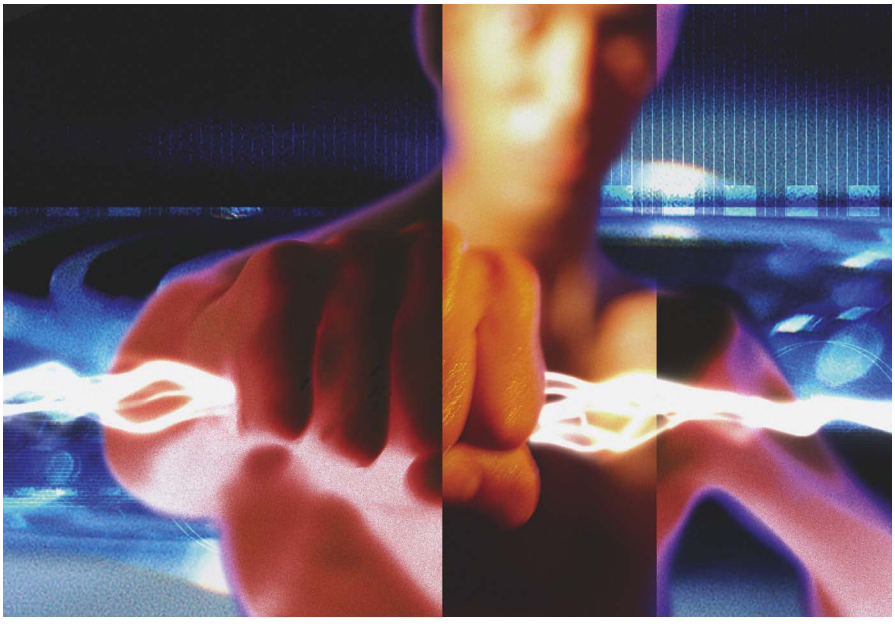


Figure 1 Cirrus Logic touts CobraNet's interoperability with other Ethernet traffic (a), and latest-generation ASSPs (application-specific standard products) come in conventional (b) and audio-DSP-core-inclusive (c) variants.

Reliable Communication in Harsh Environments



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SP3073E	1Tx/1Rx	full	500kbps	±15kV	14 Pin NSOIC
SP3074E	1Tx/1Rx	full	500kbps	±15kV	8 Pin NSOIC
SP3075E	1Tx/1Rx	half	500kbps	±15kV	8 Pin NSOIC
SP3076E	1Tx/1Rx	full	16Mbps	±15kV	14 Pin NSOIC
SP3077E	1Tx/1Rx	full	16Mbps	±15kV	8 Pin NSOIC
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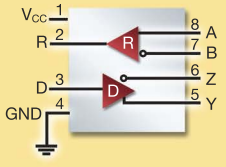
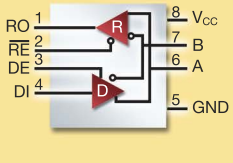
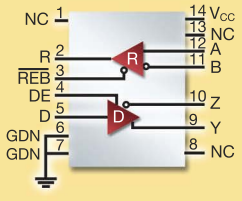


8 Pin Half Duplex



14 Pin Full Duplex



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years, but the company is waiting for a partner-developed pickup that delivers a standard of excellence reflecting MaGIC's capabilities, which include the ability to place each string on a unique audio channel.

A "SOUND" ALTERNATIVE

Digigram's EtherSound is currently CobraNet's dominant competitor. Like MaGIC, EtherSound is compatible with Ethernet at the PHY layer but requires a unique MAC. It also doesn't support traditional bus and ring topologies; instead, it requires a daisy-chain or star-interconnect architecture (based on Layer 2 switches, higher layer switches, or routers) or combinations of these two approaches (**Figure 2**). The upside of these restrictions, however, is low and deterministic latencies; an audio transfer between a master module's serial input and the next slave module's serial output is six samples—125 µsec at a 48-kHz sampling rate. Each time you add another daisy-chained EtherSound module to the path, you incur an additional approximately 1.5-µsec delay (see **sidebar** "Whither wireless?"). EtherSound is a synchronous network: The primary master module generates the network audio clock from which each downstream EtherSound device's audio clock is derived, synchronized whenever an application requires phase consistency.

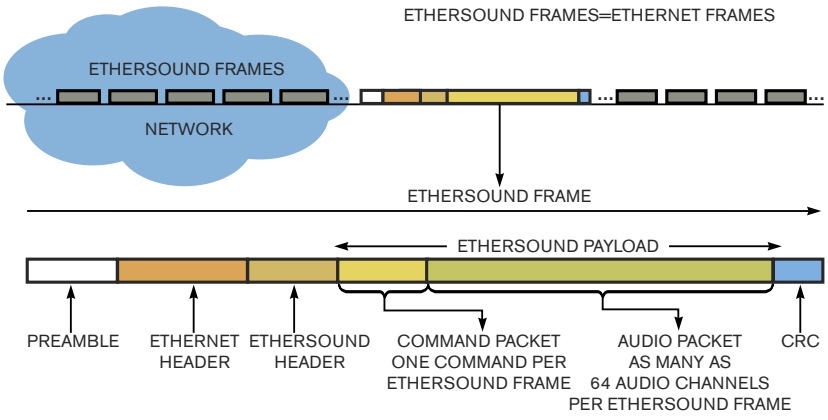

Figure 2 Each EtherSound frame combines a command packet with as many as 64 channels' worth of audio data.

Version 1.0 of the EtherSound protocol is a two-packet-per-frame approach; the first packet contains command information, and the packet that follows it contains as much as 64 channels' worth of audio information, with each channel supporting 24-bit sample sizes. EtherSound natively authorizes 44.1- and 48-kHz sample rates; audio streams at higher sampling rates—88.2, 96, and 192 kHz, for example—employ multiple channels within one EtherSound frame. A 100-Mbps EtherSound network can carry a variety of combinations of audio streams—64 audio streams at 48 kHz, for

Whither wireless?

Given that many on-stage guitar players–and, for that matter, singers and other musicians–have "gone wireless" in recent years, the idea of tethering a guitar over CAT5 (Category 5) cable seems antiquated. David Mayne, Gibson's vice president of business development for MaGIC (media-accelerated global-information carrier), points out that the company's implementation focuses on delivering low latency and maintaining 100% QOS (quality of service). Nothing inherent in the design prevents wireless transport, but wireless options fall short of the company's QOS expectations. Gibson recognizes the benefits of wireless and expects continued adoption of untethered options, but the company's first priority is quality. Chief Executive Officer and Chairman Henry Juszkiewicz refers to UWB (ultrawideband) as the "big hope," due to its comparative immunity to interference and consequent latency predictability versus today's 2.4- and 5.2-GHz WiFi (Wireless Fidelity) approaches.

Garth Wiebe, founder of AudioRail Technologies, also shares his thoughts on wireless transmission in commercial, industrial, and professional audio: "Wireless is full of pitfalls. Enter RF, and you must account for signal dropouts and retransmissions of data. This is no problem for data, but live sound cannot tolerate these. To account for them, in theory, would require large amounts of buffering, which would incur large amounts of latency, which is also unacceptable."

Expanding the discussion to video, Michael Johas Teener, a networking-system architect at Broadcom, points out, "The quality of service for wireless is not adequate for HD-quality video. Latency is excessive–tens of milliseconds–in a single-attachment-point domain, much worse in a mesh, and normal home environments can result in momentary packet loss" (Reference A). That's the reason that Belkin, for example, chose a proprietary wireless-transmission scheme based on a Magis Networks chip set for its RemoteAV transmitter-and-receiver set.

REFERENCE

A. http://grouper.ieee.org/groups/802/3/tutorial/mar05/tutorial_1_0305.pdf.

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example, or 62 audio streams at 48 kHz plus one audio stream at 96 kHz, all the way up to 16 audio streams at 192 kHz.

Materials available under license to speed your time to production include a software-development kit, source and object code, an evaluation board, and two reference designs targeting Xilinx Spartan-IIe FPGAs. Digigram also sells a number of EtherSound transmitters and receivers with various numbers and types of analog inputs and outputs, along with a the miXart 8 ES PC sound card. Planned 100-Mbit enhancements include the ability to define bidirectional daisy chains anywhere on a network, support for Xilinx Spartan-3 FPGAs, ubiquity of network management, ring-based network redundancy, and the ability to generate the network clock from any device. And, like Cirrus Logic and Gibson, Digigram is eyeing Gigabit Ethernet as a future enhancement, enabling the support of standard Ethernet components along with additional media transports, such as video and generic data.

FOCUS ON SIMPLICITY

Garth Wiebe founded AudioRail Technologies based on the premise that most people in live sound have little money to spend. He explains, "You have schools, churches, small musical organizations, theaters, conference centers, and so on. There are large sound companies and large venues, for sure, but they are dwarfed by the majority of smaller, lower budget organizations." As a result, he created the elementary M11 protocol, a 4-bit, 25-MHz data stream based on time-division multiplexing. AudioRail uses Ethernet transceivers but replaces the Ethernet MAC with a simpler FPGA-based programmable-logic design.

Figure 3 AudioRail transceivers bridge ADAT and the company's proprietary, cost-optimized MII protocol.

The result, according to Wiebe, is a reliable product that costs only a fraction of what you'd pay for other real-time-networked-audio approaches. Says Wiebe, "We have yet to have one fail in the field. Period. No customer complaints of malfunction. Period. And we have them in countries all over the world in addition to here in the United States." You can see for yourself how AudioRail's cost and reliability claims stack up to scrutiny; the company's Web site details both its and its competitors' technologies and products. Each $500 ADAT (Alesis digital-audio tape) rx32tx32 rack-mountable unit provides eight ADAT "light-pipe" optical connections, encompassing four inputs and four outputs (**Figure 3**). Each light-pipe port can carry eight 16- to 24-bit, 48-kHz audio channels for a sum total of 64 channels' worth of 24-bit, 48-kHz audio through each AudioRail dual-CAT5 link (see Brian's blog entry "Audio over CAT5: Other approaches" at www.edn.com/briansbrain).

AudioRail, like its competitors, delivers low latency: approximately 5 µsec in

Cabling choices

Is CAT5's (Category 5's) 100m specification too short for the distance you need to route audio? Consider fiber-optic cable. Cirrus Logic's CobraNet literature, for example, claims that it's possible to reliably drive a 2-km distance over multimode fiber or 100 km over single-mode fiber. Fiber-optic cable, unlike all electrical-based cabling schemes (to a greater or lesser extent), also doesn't emit an EMF and isn't susceptible to interference from other EMF-generating sources.

Additional protocols

CAT5 (Category 5) cabling's low cost and long-distance drive capability make it an attractive option for audio-data formats beyond the Ethernet-packetized variety. The MIDI (musical-instruments digital interface) Manufacturers Association, for example, is pursuing standardization of MIDI transport over CAT5, according to Analog Devices' DSP Marketing Programs Manager (and formerly corporate marketing manager at MIDI software provider Staccato Systems) Denis Labrecque, although association representatives didn't respond to requests for information, and the association's Web site currently lists only MIDI-over-IEEE-1394 specifications.

FireWire-encoded audio over CAT5 cabling is another possibility, one that FireWire audio pioneer Bob Moses is pursuing with his latest venture as vice president and director of engineering of Wavefront Semiconductor. Moses comments, "As far as I know, I'm the only guy to have built an audio-over-CAT5-using-Firewire box, so far. Actually, I've built two. The first was a reference design called OnRamp using TI silicon. The second reference design is the evaluation module for our new Dice II FireWire audio chip...We plan to send 400 Mbps down CAT6 (or 200 Mbps down CAT5e or 100 Mbps down plain-old CAT5). We believe that this solution is much cheaper than an Ethernet solution, and you get all the benefits of FireWire isochronous transport, which you do not get with the other audio-over-Ethernet solutions."

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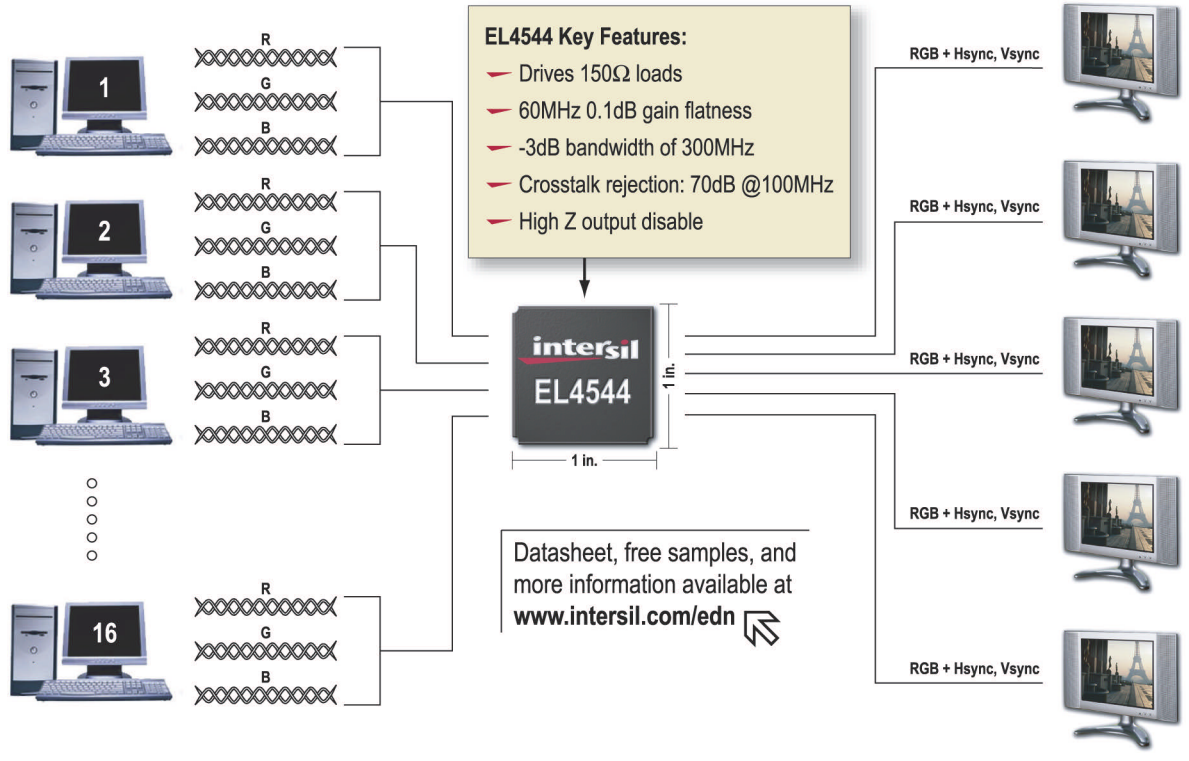

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the digital domain—more precisely, 4.5 µsec+0.25 µsec/hop+0.005 µsec/m, end to end. Wiebe warns, "One feature ... that provides flexibility and versatility but can cause a nuisance is that AudioRail digital-audio streams are all independently clocked to follow their source. AudioRail can be simplistically modeled as a bundle of digital-audio cables taped together. They do not have a common clock. The flexibility and versatility mean that you can run clocked domains at different sample rates through the same CAT5 cable. The potential nuisance part ... is that, if you have only a single digital-audio system, you must make sure that all devices are properly slaved off of a clock master, even though they all come from the same AudioRail box. This can mean a little extra strategizing and perhaps a few extra-short-word clock BNC cables at each end to tie the devices' clocks together." EDN

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2. www.gibsonmagic.com/MaGICfaq.pdf.

ACKNOWLEDGMENTS

Thanks to Garth Wiebe, founder of AudioRail Technologies, for his in-depth background on digital-audio-transmission history, to both Wiebe and Michael Johas Teener, a network-systems architect at Broadcom, for their information on current audio-over-CAT5 alternatives, and John Strawn, principal consultant and owner of S Systems, for his efforts in connecting me with various individuals and companies associated with this article's topics.

AUTHOR'S BIOGRAPHY

Technical Editor Brian Dipert longs for a world filled with fiber-optic cable, ultrawideband wireless, and instant-response, blazingly fast servers on the other end of his network connection. Oh, and world peace. A guy can dream, can't he?

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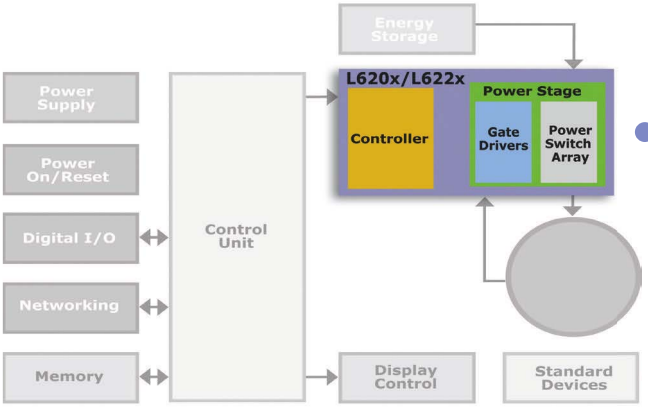

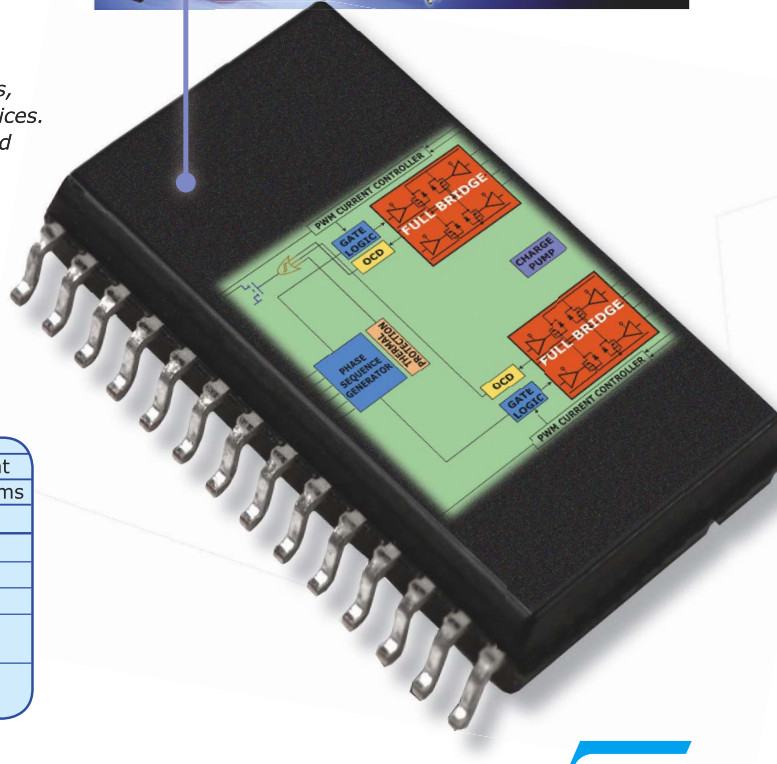

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BY MAURY WRIGHT • EDITOR AT LARGE

WHICH INTERFACE WILL GET TRACTION?

FIBRE CHANNEL RULES IN THE SAN WORLD, AND INFINIBAND IS PROGRESSING IN COMPUTER CLUSTERS, BUT A FASTER FLAVOR OF THE VENERABLE ETHERNET LOOMS AS A POTENTIAL JACK-OF-ALL-TRADES.

ILLUSTRATION BY JAMES GARY

Typical enterprise IT departments now support three networks. Ethernet links PCs and servers. FC (Fibre Channel) connects SANs (storage-area networks) that connect servers to storage arrays. And proprietary interconnects, Myrinet, or emerging IB (InfiniBand) technology generally link clusters of servers that focus on evolving multithreaded tasks, such as database access. For board and system designers, however, that landscape may change significantly. Proponents believe that IB will first prevail in clusters and then move into storage applications, whereas proponents of 10 GBE (10-Gigabit Ethernet) believe the LAN technology will win in each segment. And you aren't immune to this changing landscape if you don't happen to design servers or storage products. The interconnects that win in these applications will find use in all sorts of specialty applications driven by the low-cost ICs that volume deployment in the enterprise invariably delivers.

A little more than a year ago, Broadcom launched what it termed C-NIC (converged-network-interface-controller) ICs (**Figure 1**) and squarely targeted Ethernet to replace FC, IB, and proprietary technologies in storage and cluster applications. The theory goes that iSCSI (Internet Small Computer Systems Interface), an IETF (Internet Engineering Task Force) standard, provides the means for moving block-storage data across a TCP/IP (Transfer Control Protocol/Internet Protocol) network and remotely managing storage resources. Meanwhile, RDMA (remote-direct-memory-access) extensions to TCP/IP, an RDMA Consortium standard, support both iSCSI block operations and the low-latency copy of data from one system to another that clusters require. Ethernet still may lack the performance these applications require, but TOEs (TCP/IP-offload engines) and similar technologies can fix that problem.

This time is far from the first that anyone has applied a flavor of Ethernet and TCP/IP to an application in which it seemingly doesn't belong. Embedded systems regularly use low-cost Ethernet chips to link relatively unsophisticated sensors and control systems. EPON (Ethernet-passive-optical-network) technology is one flavor of fiber-based broadband that carriers are deploying to support the so-called triple play and IPTV. System builders have even used Ethernet for board-to-board communications over backplanes in systems based on buses such as CompactPCI. Another fabric, the Advanced Switching Interconnect, may replace Ethernet in the system-fabric role (see **sidebar** "Understanding the Advanced Switching Interconnect"). All these interconnects have their own places in the computer-architecture puzzle (**Figure 2**). Rick Maule, chief executive officer of start-up Ethernet-chip vendor NetEffect, states, "We believe that there is truth to the adage: 'If Ethernet can Ethernet will.'" In the case of storage and cluster interconnects, Ethernet is an attractive option for several reasons. For starters, IT departments could potentially use one set of network-management tools if the departments base data, storage, and clustering all on Ethernet—even if they actually implement them on physically separate Ethernet LANs. Assuming that the ramp in Ethernet is true to form and 10 GBE becomes a high-volume technology, then surely it will be cheaper than FC, IB, or other options. And Ethernet might carry a mix of data, cluster, and storage traffic on a single network.

ENTERPRISE NIRVANA

Tim Golden, director of PowerEdge-server marketing at Dell, states, "The notion of fat pipes and a single fabric—it's a very promising thing." Golden claims that, from an IT perspective, nirvana might be "a cloud with all resources that can be managed from a single remote point." Broadcom's C-NIC marketing material was the first to make that pitch.

So, Ethernet wins, right? Not so fast. The best effort packet-delivery and collision-based MAC (media-access-control) scheme of Ethernet and TCP/IP isn't a perfect match for storage and cluster applications that demand low latency and guaranteed quality of service. Moreover, low cost—when it comes to 10 GBE—isn't a sure thing.

First, consider cost. Through 1 GBE (1-Gigabit Ethernet), you could easily identify applications that would almost ensure broad market adoption of the next-generation technology. Today, vendors ship almost all clients with 1-GBE ports, although enterprises haven't performed wholesale upgrades of their switches and routers. Still, applications such as video delivery will lead to ubiquitous 1 GBE. But it's tougher to make a case for 10 GBE even if the chip vendors can drive down the cost of 10 GBE using process-geometry reductions.

Most of the Ethernet proponents point to the "if-you-build-it-they-will-come" nature of the tech industry when it comes to data rates and memory. But for 10 GBE, it may be tough to identify any application that requires the sheer data rate the technology affords. Instead, the justification may ultimately be how quickly you can move a large data file—say, a full-length movie—across a network that drives adoption rather than just the ability to stream live movies.

Broadcom sees the process as self-prop-

AT A GLANCE

- With volume sales driving down Ethernet's implementation costs, customers are adopting it in applications in which it seemingly doesn't belong.
- Ethernet and TCP/IP lack the performance characteristics that storage and clusters require, but extensions such as TOE, RDMA, and iSCSI can close the performance gap with interfaces such as IB.
- Unlike earlier generations of Ethernet, 10 GBE (10-Gigabit Ethernet) may not ramp quickly to volume deployment because it's difficult to find applications that require the faster data rate. Then again, the tech industry always seems to find a need for more memory and bandwidth.
- Fibre Channel may well remain the dominant choice in storage networks, despite the attack from both 10 GBE and IB.

agating. Allen Light, senior product-line manager for C-NIC, acknowledges that his company is just now getting people to move to 1 GBE. But Light claims that virtually all servers that companies ship today have dual 1-GBE ports. He claims that IT managers will soon discover and start using the available excess bandwidth for storage applications. The transition of storage traffic will lead to greater traffic demand and ultimately to volume deployment of 10 GBE. Maule of NetEffect claims that server designers adopt each succeeding Ethernet generation when the price premium is two or three times the cost of the previous generation—essentially "future-proofing" the design. Maule states, "The server deployment gets you the several-million-unit volume that drops the premium to 30 or 40%, and that then gets you into clients."

UNDERCUTTING PRICES

Ironically, IB is far cheaper today despite the fact that low cost is Ethernet's normal calling card. Mellanox Technologies is the only true merchant supplier of IB chips. Topspin Communications had developed both IB chips and system-level products, such as IB switches. But Cisco acquired Topspin and uses the company's ICs only internally in IB switches and other products. PathScale also developed an IB ASIC that it uses on board-level products. It's unclear whether the company will pursue chip-level business. Still, Mellanox has driven chip prices to less than $100. The InfiniHost III Lx chip it announced in March costs as little as $69 in high volume, and dual-port chips sell for approximately $200. Ted Rado, vice president of marketing at Mellanox, claims that his company has shipped 500,000 IB ports and that it shipped 300,000 of those 500,000 in the past year. Rado puts 10-GBE shipments at less than one-tenth that volume, pointing out that IB is enjoying the volume advantage for now.

Debbie Vogt, vice president of marketing at Ethernet proponent Siliquent, doesn't dispute the current IB cost advantage. Siliquent claims to be the first company shipping 10-GBE chips that can support storage and cluster applications. And Vogt admits that the 10-GBE links—the chip on both ends and the cable that connects the two—cost three to four times as much as an IB link today. Still, Siliquent officials believe that Ethernet is the future for clustering and storage. Vogt states, "Being able to do something with IP throughout an infrastructure is very powerful."

In reality, the cost comparison also goes far deeper than the NIC price. Ultimately, you must factor in the cost of switches and other infrastructure. As Broadcom's Light states, "You do TOE, RDMA, and iSCSI only on the ends," meaning that standard 10-GBE switches will handily carry storage and cluster traffic and will likely cost far less than IB switches.

ENTRENCHED CONTENDERS

Cost is obviously only one point of comparison. You also need to evaluate how Ethernet and the competition stack up from a performance perspective. In the storage segment, FC is the entrenched competitor. Originally a 1-Gbps interconnect, FC is now widely available at 2 Gbps, and the industry is doing early testing of 4-Gbps products. FC's developers designed it with a relatively thin protocol layer for the block-level data-storage and -manipulation requirements of big databases, such as Oracle. The interconnect also finds use in storage-centric applications, such as data mirroring and transparent backup and restoration. For more background information, check out the Fibre Channel Industry Association's Web site.

In the cluster case, the installed base is more diverse. Some of the "big-iron" computer vendors have proprietary interconnects. Mellanox boasts a number of impressive case studies of IB-based clusters; you can find details on the company's Web site. At a signaling rate equivalent to that of 10 GBE, IB delivers 8-Gbps data rates due to the 8B/10B encoding that IB uses. IB is scalable through the addition of signaling lanes, and supporters are planning a doubling of data rates, but the 8-

(continued on pg 64)

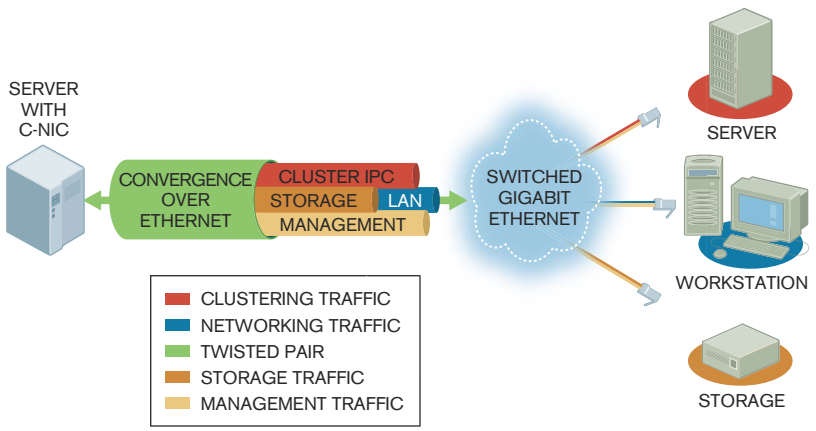

Figure 1 Broadcom has evangelized the convergence of data, storage, and cluster interconnects since the announcement last year of its C-NIC family.

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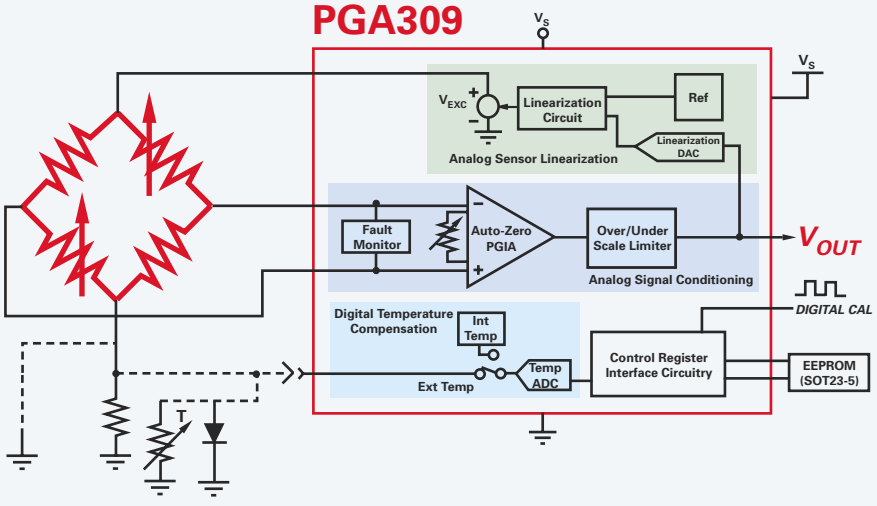

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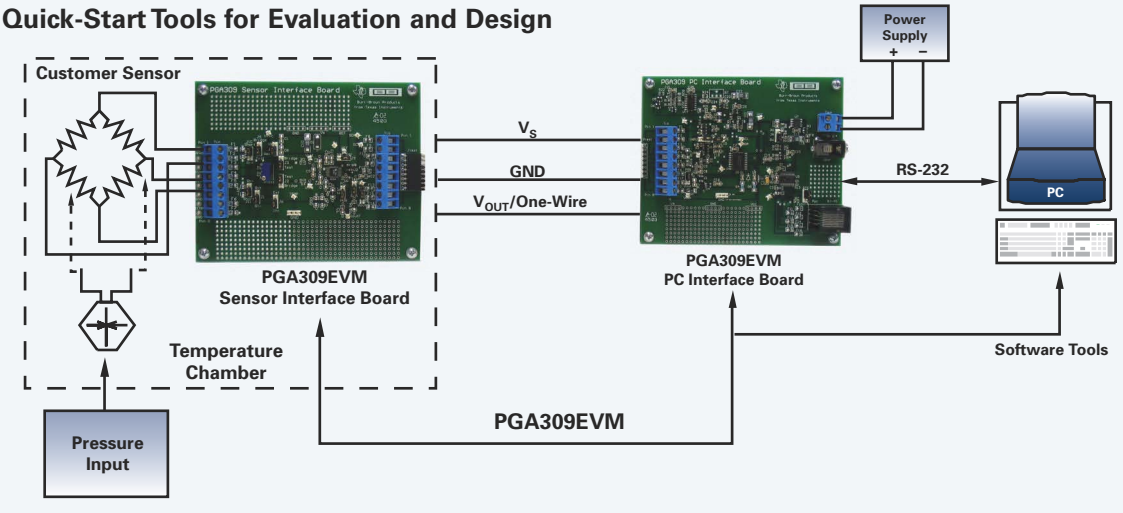

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UNDERSTANDING THE ADVANCED SWITCHING INTERCONNECT

By John Chiang, IDT

The ASI (Advanced Switching Interconnect) serial-interconnect technology provides high-performance features of proprietary fabrics and uses the standards-based economy of scale and ecosystem of PCI Express.

Through enhancements in the transaction layer, ASI extends the capabilities of PCI Express to support a variety of converged computation and communication applications (Figure A). Key features of ASI include low latency, peer-to-peer communications, multiple levels of QOS (quality of service), sophisticated congestion management, high reliability and fail-over mechanisms, multiprotocol and multicast support, and built-in security. ASI targets backplane and local onboard-interconnect applications, as well as chassis-to-chassis communications.

ASI provides as many as 20 virtual channels, of which eight are bypass channels that can transport load and store protocols, eight are ordered only, and four are multicast, to facilitate almost any application profile. At the logical level, it supports eight traffic classes per virtual-channel type for QOS and traffic differentiation. ASI uses a credit-based, link-level, flow-control scheme. For congestion management, it supports status-based flow control, injection-rate control, minimum bandwidth, or vendor-defined egress scheduling.

ASI embraces compatibility and provides the mechanisms for more efficiently supporting legacy infrastructure. It realizes this goal through various native data-movement protocols, software semantics, and protocol-agnostic tunneling through a universal fabric technology. PI-2 (protocol interface 2), generic data transport, provides a reliable transport mechanism with built-in segmentation and reassembly for message-passing architectures. Users can employ it to interoperate various endpoint devices, such as NPUs (network-processing units), CPUs, microprocessors, and DSPs. ASI defines PI-0 to PI-95. It leaves PI-96 to PI-127 for vendors' proprietary protocols. It assigns the protocols as follows:

- PI-0: spanning tree,
- PI-1: congestion management,
- PI-2: generic data transport,
- PI-4: device management,
- PI-5: event reporting,
- PI-8: PCI Express tunneling,
- PI-E: Ethernet tunneling,
- PI-9: socket-data transfer,
- PI-10: simple load store, and
- PI-11: simple queue (SQ).

ASI has not yet assigned PI-12 through -95.

Fabric-management capabilities are also part of the ASI protocol to support a number of services, such as connection setup and teardown, event management, performance and health monitoring, redundant routes, path invalidation, resource allocation, and load balancing.

ASI provides a scalable architecture by using the same PHY (physical) and data-link layers as PCI Express. It supports 2.5-Gbps serial-link technology in one-, two-, four-, eight-, 12-, 16-, and 32-lane configurations. Second-generation, 5-Gbps serial-link technology has also emerged. ASI can flexibly autonegotiate and interoperate to a variety of port bandwidths that different applications require. It also supports lane reversal to prevent a failure of a single lane's bringing down the entire link. ASI supports various fabric topologies, such as meshed, star, dual star, and dual-dual star and can cascade to larger fabric topologies by integrating sophisticated congestion-management and end-to-end flow-control capabilities.

ASI targets enterprise, communications, and embedded systems requiring high-performance fabric features. Typical applications include enterprise storage routers and arrays; blade servers; telecom edge, access, and metropolitan switches and routers; and embedded-system computing, such as in military and medical imaging. ASI works with any protocol and its broad industry support and maturing ecosystem of products provide strong advantages over proprietary- or niche-fabric technologies.

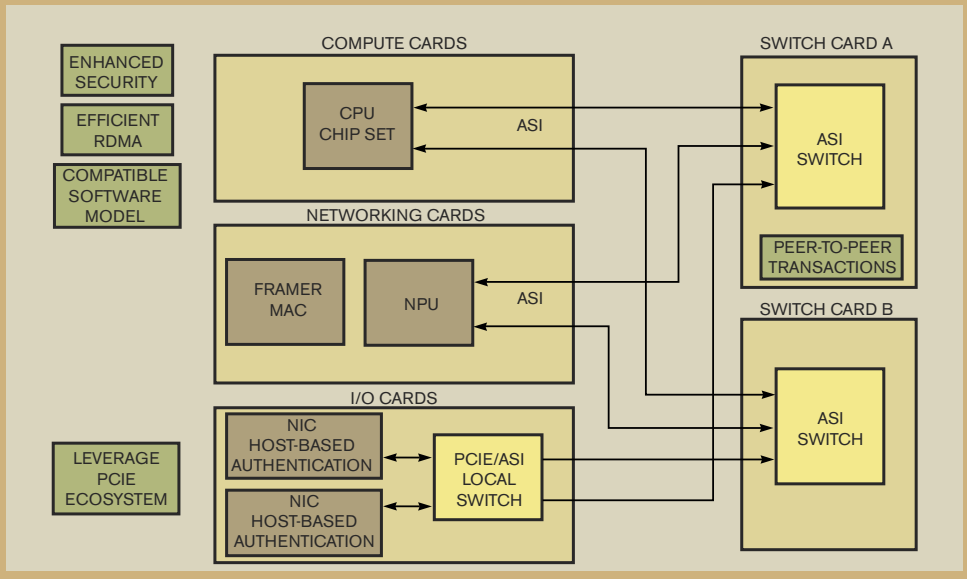

Figure A Through enhancements in the transaction layer, ASI extends the capabilities of PCI Express to support a variety of converged computation and communication applications.

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John Chiang is product manager of IDT's Serial Switching Division.

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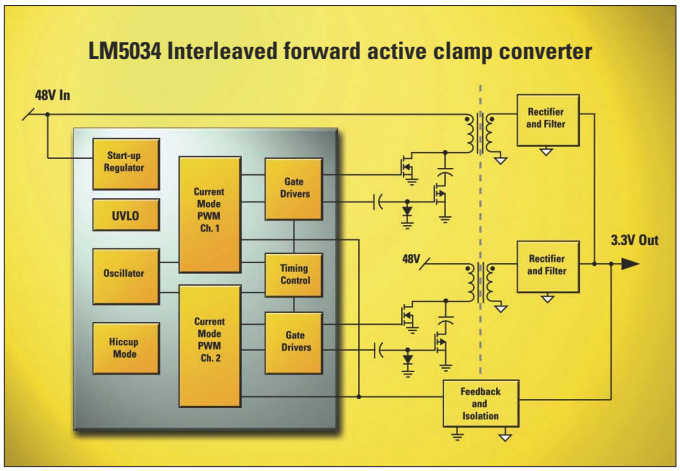

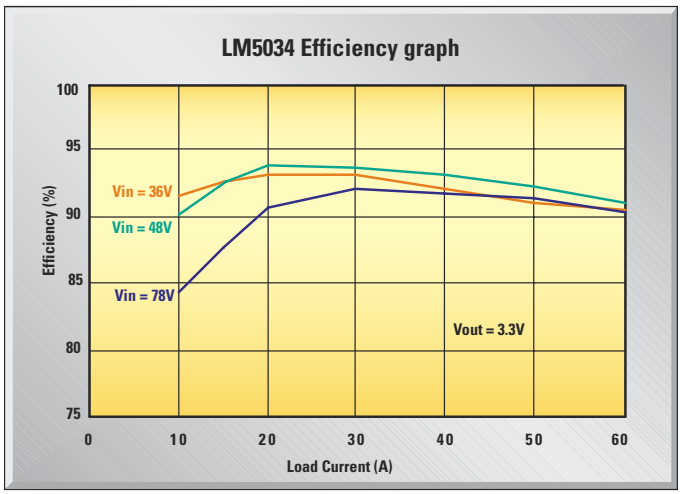

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Gbps flavor is likely to find the broadest near-term use. Visit the InfiniBand Trade Association for more background.

Still, the volume of IB cluster installations is relatively small compared with total cluster deployments. Most deployed, nonproprietary clusters now use Myrinet technology from small, privately held Myricom. The company supplies Myrinet host adapters and switches to most of the major server vendors, including Hewlett-Packard, Sun, and IBM. The Myrinet technology that's now available is a full-duplex, 2-Gbps PHY (physical layer) and a set of routing and link specifications that ANSI has standardized. Myricom adds a proprietary set of protocol and software layers for clustering.

You can get a quick look at leading-edge cluster deployments at the Top500 Supercomputer Sites' Web site. The site biannually releases a new list of the most powerful high-performance-computing installations in the world. If you select the database tab, you can sort the data by interconnect type, and you will see the success that Myrinet enjoys. But note that the categorization is imperfect because it classifies at least a few systems that have "IB" in some form as having "mixed" interconnects, and some Myrinet systems may suffer the same fate.

In any event, it's clear that Myrinet, IB, and FC all have data-rate advantages over 1 GBE. Still, Broadcom believes that a lot of 1-GBE business exists in storage and clustering, and the company seems in no hurry to announce 10-GBE products. But most believe that success for Ethernet will require a move to the faster 10-GBE flavor. And the equally challenging issue for Ethernet is the latency and best effort service of both Ethernet and TCP/IP.

LATENCY IS KEY

Many ways exist for defining, specifying, and benchmarking latency, and little consistency exists when it comes to interfaces and types of networks. Still, FC products regularly claim latency of less than 1 μsec. Both Myrinet and IB also offer latencies of much less than 5 μsec and into the 1- to 3-μsec range. Standard Ethernet networks feature latencies greater than 50 μsec and even up into the hundreds of microseconds.

The latency limitation associated with Ethernet comes from both the collision-based MAC protocol and TCP/IP. TCP/IP in fact affects the situation in two ways. TCP/IP allows out-of-order packet processing and reassembly after delivery. And TCP/IP is so complex that data delivery requires significant processing overhead.

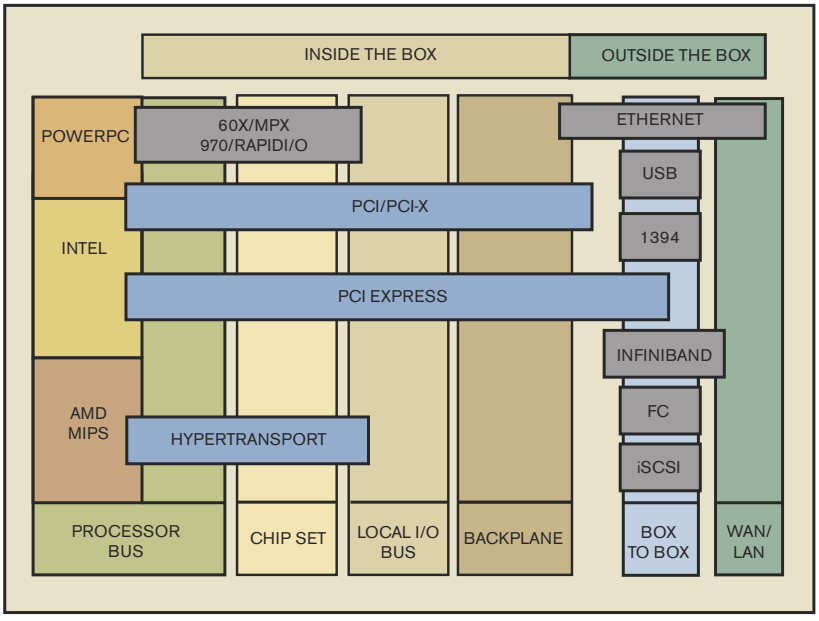

Figure 2 Various computer-interconnect technologies fit into various niches, although users have shoehorned Ethernet into may places other than LANs (courtesy PLX Technology).

IB proponents, such as Mellanox, claim that, at 10-GBE rates, a host processor can spend as much as 90% of its time on TCP/IP processing. Mellanox's Rado claims that the company's IB chips, running at full wire speed, require only 3 to 4% of the CPU's cycles for overhead. Chuck Seitz, chief executive officer of Myricom, makes an even more astounding claim. According to Seitz, two Myrinet systems can transfer a 1-Mbyte block of data from user memory on one system to user memory on another system, and the two system CPUs cumulatively spend 0.3 μsec on the transfer.

Engineers and IT specialists have long understood the problem of Ethernet-protocol complexity. In the days of 16-bit CPUs, an Ethernet card dedicated a processor to the TCP/IP tasks. Over time, host CPUs became sufficiently powerful that TCP/IP became a host's insignificant chore. Now, with the move to 1 GBE and then 10 GBE, TCP/IP overhead has again become an unacceptable burden on host CPUs in many applications and an issue that storage or cluster networks must face.

These days, chip vendors are integrating TOEs into their products to reduce the impact of the protocol. In fact, all of the Ethernet proponents, including Broadcom, NetEffect, Siliquent, and Astute Networks, list TOE as a standard feature. But TOE alone will not make Ethernet an effective storage or cluster fabric. Maule of NetEffect claims that packet processing associated with TCP/IP is responsible for only about 35 to 40% of the total overhead associated with Ethernet. Maule claims that tasks such as intermediate buffer copies are responsible for 20 to 25% of the overhead. And he adds that operating-system overhead—moving into and from kernel space and handling interrupts—can be responsible for as much as 40% of the overhead. Maule states, "You must reduce overhead by 90% or more."

Maule points to the new iWarp, or high-speed-Internet, standard as the answer. The standard builds on RDMA and TOE, and a consortium at the InterOperability Laboratory at the University of New Hampsire Research Computing Center is nurturing it. The iWarp standard enables an "operating-system-bypass" technique that allows applications running on two computers to exchange data blocks with no intervention from the operating system. Maule claims that TOE handles the protocol overhead; RDMA, the buffer-copy problem; and iWarp, the operating-system issues.

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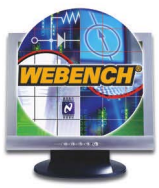

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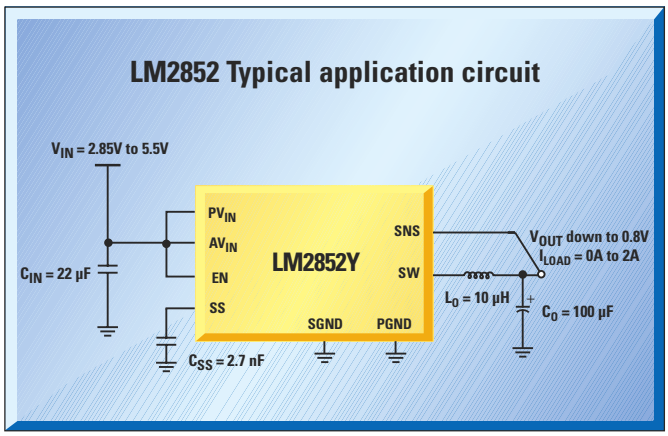

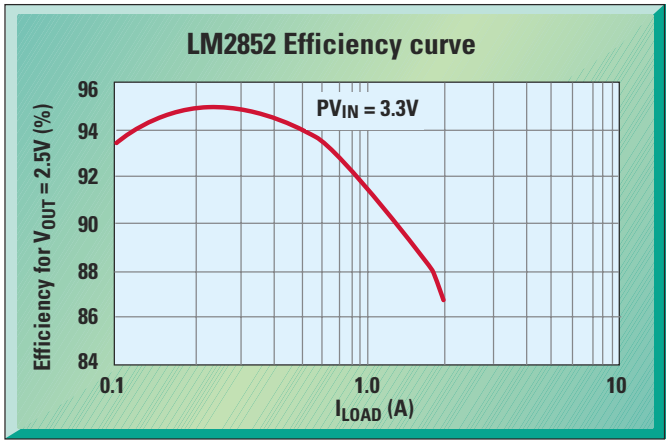

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a full year ago. The $500 SLQ1010 and the 4-Gbps SLQ1004 are available, but Siliquent can't yet claim that equipment vendors are shipping products based on the chips. But the company's Vogt expects customer shipments to begin shortly. She claims that the chips fully support iWarp and that latency with iWarp is now less than 10 µsec. Moreover, she believes that they will get to 5-µsec latencies.

Meanwhile, NetEffect last November announced an iWarp product, but Maule admits that the chips have yet to ship but promises them this year. You can now buy 10-GBE board-level products with TOE capabilities. Both Neterion (formerly, S2io Inc) and Chelsio have such products, although neither now claims iWarp support. Hewlett-Packard has begun to ship products based on the 1-GBE Broadcom BCM5706 and to espouse the converged-network philosophy. Broadcom also has a 2.5-Gbps version of the C-NIC family available.

Astute Networks may have been further along the 10-GBE chip-development path when a year ago it demonstrated the Pericles chip based on 10 Tensilica RISC cores. But that first chip included SPI-4 (System Packet Interface, Level 4) interfaces and targeted the system side of the 10-GBE link. The company has since refocused on the storage-appliance side of the SAN application and is working on its next-generation offering. Jon Siann, Astute's vice president of marketing, claims that the company learned the hard way that TOE and RDMA support is insufficient to win customers. The company's experience yielded the decision to focus on SANs in which Astute will deliver complete sets of storage software, such as mirroring and data-migration applications. Siann does not believe that one IC design can succeed in both the cluster and the storage segments. "You are not going to win both," he says.

In the short term, designers may have no choice but Myrinet and IB for clusters and IB and FC for storage. Despite many pro-Ethernet statements, Dell's Golden states, "For the next few years, IB may be the best thing going." IB does seem to be on a roll. Mellanox's Rado goes so far as to say, "I challenge the theory that Moore's Law can eliminate the TCP/IP-overhead problem of Ethernet." Mellanox officials believe that, at the very least, the silicon needed to offset the disadvantages of Ethernet will keep IB prices in an advantageous position. Moreover, Rado points out that IB will double rates before 10 GBE can come down the cost curve.

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Read more of what Maury has to say on many topics at his blog, www.edn.com/ontheverge.

An announcement that should occur just before press time, slated for the International Supercomputer Conference in Heidelberg, Germany, might change things, however. Myricom is planning the next generation of Myrinet: Myrinet-10G. The 10-Gbps technology will migrate to the 10-GBE PHY and maintain Myricom's clustering-protocol and software layers. Essentially, the most common clustering technology in the market will be faster than IB.

Myricom plans to launch the technology at aggressive prices. NICs will sell for $795, and switches will sell for $400 per port. Moreover, the new ICs that the company developed for the launch can run either the Myrinet protocols or TCP/IP, so the new products can carry Ethernet traffic. Myricom has always assigned Ethernet MAC addresses to its products and uses what appear to be standard Ethernet drivers to support the products. The Myrinet-10G launch will also make Myricom a full-fledged chip supplier.

Chief Executive Officer Seitz claims that Myrinet has a huge advantage over IB. He states, "For InfiniBand, RDMA is not only not the answer; it's part of the problem." He claims that the IB standard is flawed when it comes to how RDMA is implemented and that the flaw both drives up memory requirements and hurts performance because an application cannot move blocks of data from user space in one machine to user space in another. NetEffect's Maule essentially concurs. NetEffect began life as Banderacom, an IB player, and company officials believe the lessons it learned in IB serve it well in pursuing iWarp. Maule claims that IB has a user-level direct-access problem.

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On the storage side, meanwhile, it's a fair question to ask why FC needs a replacement. One theory holds that TCP/IP-connected Network Attached Storage (NAS) appliances are far cheaper than SAN systems, and iSCIS enables remote management of and access to NAS appliances. Still, even in the SAN environment, SAS (Serial Attached SCSI) or SATA (Serial ATA) will shortly replace the native FC-based drives vendors are deploying in SAN boxes today. The FC fabric of a SAN differs from the FC loop in a drive array at the PHY level, but the two share the storage protocols. As the drives move to SAS, momentum will likely emerge to migrate away from FC because it will become yet another bridge interface in enterprises. Still, it's tough to find anyone other than Mellanox that believes IB will take over the SAN, and FC may be a healthy market for years. EDN

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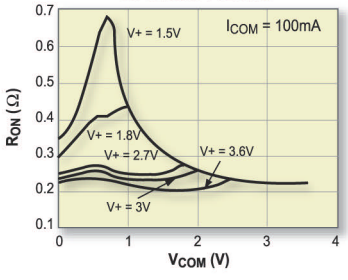
Singles	ISL84714	SPDT/2:1 Mux	0.44	0.06	6kV	1.6 to 3.6	SC70-6
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP

ISL84684 Typical Performance

ON RESISTANCE vs. SUPPLY VOLTAGE vs. SWITCH VOLTAGE



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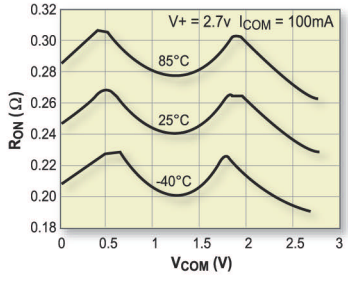

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Structured ASICs deserve serious attention at 90 nm

THE COST OF 90-NM—NOT TO MENTION 65-NM—SILICON IS OUTRAGEOUS. USERS SHOULD TAKE A LONG, HARD LOOK AT STRUCTURED ASICs WHEN CONSIDERING WHICH FABRIC TO USE FOR THEIR NEXT LOGIC DESIGN.

Four years after ASIC vendors introduced their first structured-ASIC devices in response to FPGA vendors eating up their market share, the structured-ASIC market has yet to become a popular choice for logic designs.

But analysts say that the structured-ASIC market is a viable business today and may exceed $1 billion by 2008, as designers add up the cost of 90-nm ASIC design and run up against the hard limitations of FPGAs.

Analysts and structured-ASIC vendors put up good arguments about why you should at least consider structured fabric for your next IC-design project. But you should consider a number of variables—both technical and business—when evaluating FPGAs, structured ASICs, and cell-based ASICs.

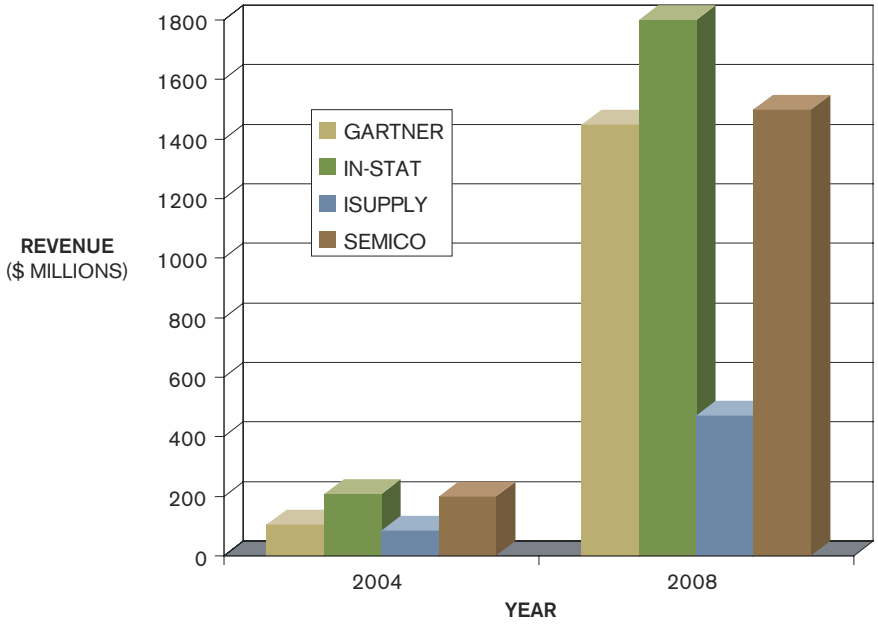

Figure 1 Semiconductor analysts say that the structured-ASIC market isn't going away.

Companies market structured ASICs as the midvolume, midprice missing link between fast-turnaround, reprogrammable but low-volume FPGAs and high-cost, high-volume, hard-to-design cell-based ASICs.

A structured device resembles a gate array on steroids. Like gate arrays, structured ASICs have a limited number of designable layers (usually one to six), a low tool and NRE cost, and a turnaround time ranging from days to months. As with gate arrays, silicon vendors have taken care of most of the nasty physical-design effects with prerouted and pretested layers. In most devices, they've also predesigned the clock tree. But structured-ASIC devices offer much larger designable gate counts and much more on-chip memory than gate arrays.

A VIABLE MARKET?

The structured-ASIC market has not yet seen widespread adoption among users and has not yet become the $300 million market many proponents had predicted. FPGA proponent Tom Hart, CEO of Quicklogic, goes so far as to say, "Structured ASIC is the last dying gasp of the ASIC business," and John East, president and CEO of Actel, says that structured ASIC "suffers from the same drawbacks that have caused ASICs to lose market share to programmable devices over the past two decades."

Many analysts, however, disagree with Hart's and East's assessments of the structured-ASIC market, saying that FPGAs, structured ASICs, and cell-based ASICs all have unique functions and their own place in the logic-device market.

"This is not about who is going to win," says Semico Research Corp's senior ASIC and SOC (system-on-chip) analyst Richard Wawrzyniak. "It is about what combinations of features and functions, power, time to market, and cost best suit your needs."

Although the structured-ASIC market posted 2004 revenue ranging from only $86 million (iSuppli) to $209 million (In-Stat), not $300 million as previously expected, the market, say analysts, shows signs of picking up (**Figure 1**).

Research company IBS Inc predicts

AT A GLANCE

- The structured-ASIC market has yet to produce big revenue, but analysts say that it may be the best bet for complex and midvolume designs.
- The cost of 90-nm silicon and the hard limitations of FPGAs will boost the structured-ASIC market past the $1 billion mark by 2008, analysts say.
- A 90-nm ASIC costs anywhere from $30 million to $50 million to produce.
- Structured ASICs have NREs of $0 to $250,000, low to no tool cost, and turnaround times of days to weeks, giving them lower engineering and overall costs than traditional ASICs.
- When it comes to volume, FPGAs are the right choice to 20,000 units, and structured ASICs are the right choice for 100,000 to 3 million units. Traditional ASICs still have the strongest play at greater than 3 million units.

that by 2007, one-third of all ASICs will employ structured-ASIC fabric. Bryan Lewis, research vice president and chief semiconductor analyst at Gartner, more or less concurs.

"By 2008, structured ASIC will be about a third of the designs out there, but the revenue is less than 10% of the overall ASIC market," he says. "For a structured ASIC, the typical revenue per design is running around $3 million or $4 million, and in a traditional ASIC, it is running at $5 million or $6 million."

Lewis believes that the structured-array market, which in 2004 was worth $104 million, will become a $1.45 billion market by 2008, with design starts moving from 181 in 2004 to 1230 by 2008. He believes Altera and LSI Logic are currently the structured-ASIC market leaders. He says most structured-ASIC vendors, with the exception of Altera, have been tightlipped when asked about revenue. He notes that Altera reported $19 million in revenue from its HardCopy structured family in 2004. Altera was the only company to provide tapeout and customer data for **Table 1**.

Alain Bismuth, vice president of the HardCopy product group at Altera, says that the company's customer base for HardCopy has increased from 20 to 30 customers over the last year and that there were 12 design starts in 2003 and 20 in 2004. In 2005, the company has doubled capacity to accommodate growing demand for structured ASIC.

"We exited 2004 with one tapeout a week, and so as we entered 2005, we decided to double our capacity," says Bismuth. "This means we can now accommodate 100 tapeouts per year. We did this to support growth across all market segments."

Simone Shaghafi, ASIC-marketing manager at Fujitsu Microelectronics, says that Fujitsu customers are also showing increased interest in the company's structured-ASIC lineup.

"For the past six months, over 70% of the RFQs [requests for quotes] we have received are for structured ASICs," says Shaghafi, noting as does Bismuth that the main reason for customer interest in structured fabric is the rising cost of ASIC and hard limitations of FPGA fabric.

"At 90 nm is when this industry will really kick in," says Lewis.

AFFORDABLE DESIGN?

At 90 nm, an ASIC mask costs more than $1 million, and, as the process matures, the industry expects that cost to drop to approximately $750,000. That's still roughly twice the cost of a 0.13-micron mask when vendors introduced that process. When TSMC announced its 65-nm process earlier this year, its officials said that the normalized cost of a TSMC mask would cost approximately $1.5 million. Meanwhile, IBM and Chartered Semiconductor say that the initial cost of a 65-nm mask will likely be well over $2 million.

AT 90 NM, AN ASIC MASK COSTS MORE THAN $1 MILLION, AND, AS THE PROCESS MATURES, THE INDUSTRY EXPECTS THAT COST TO DROP TO APPROXIMATELY $750,000.

It's especially disconcerting considering that a given design group's next design will likely require more than one mask set and maybe a few mask sets simply because design complexity continues to increase at the 90-nm node.

Designs at 90 nm, say vendors, require more functional verification than 130-nm designs. They also require extra steps in physical design, such as optical proximity correction for all layers, resulting in higher engineering cost. The tools to handle these advanced process effects and verification also are becoming more expensive.

Thus, analysts estimate the total development cost for a 90-nm ASIC will run anywhere from $30 million to $50 million, with the bulk of that cost coming from engineers designing and verifying the functions of the design.

That lofty price, say analysts, will limit the number of designs targeting that node to high-volume applications, such as cell phones, game consoles, graphics ICs, and automotive products.

HARD LIMITATIONS OF FPGAs

FPGAs' instant reprogrammability and in-circuit verification have made them invaluable in any designer's toolbox. Over the last two decades, FPGA vendors have made leaps and bounds in reducing the volume cost of their devices. At the same time, they have increased gate counts and device performance and in turn annually taken over more of the ASIC business. Designers no longer use FPGAs just for ASIC prototyping. Each year, FPGA vendors offer more gates at prices that make devices reasonable for high-volume use.

Semico's Wawrzyniak says that FPGA has grown into a $3 billion market, which is one-third smaller than the ASIC market, at $9 billion, he estimates.

But although FPGAs have improved on all fronts, even the highest end FPGAs don't have the density, performance, and especially the midvolume and high-volume unit costs of ASICs, which are 10 times less expensive than high-end FPGAs at volume, analysts estimate.

FPGAs also have hard limitations and are unsuitable for use in wireless designs, especially cell phones, which require very low power, small die/package size, extremely large gate counts, and top performance.

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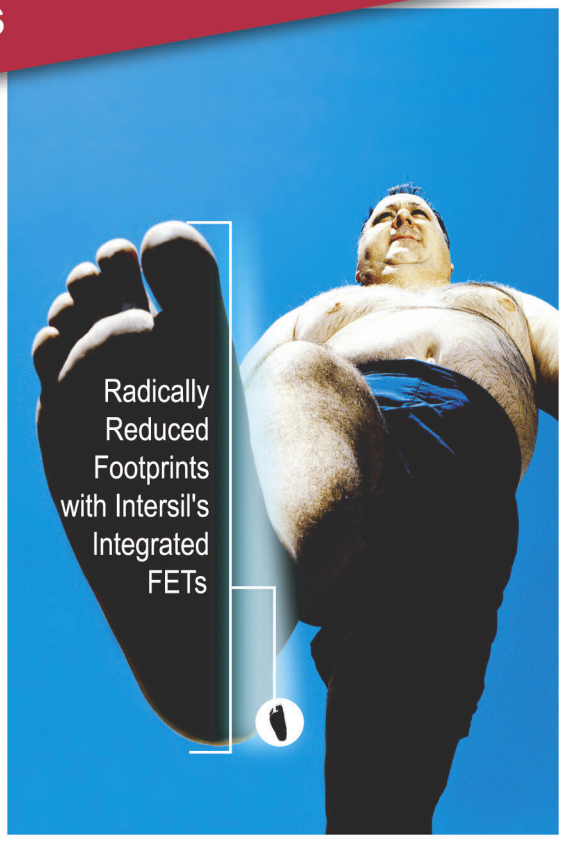

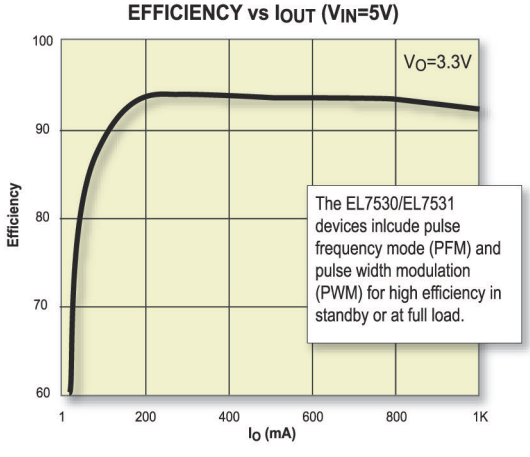

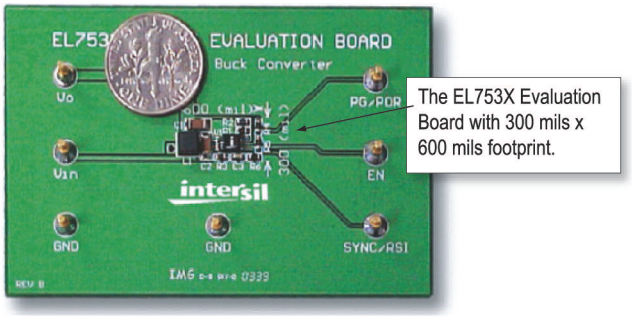

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FPGAs use more transistors than do structured or cell-based designs for functions other than logic, says Ronnie Vasishta, executive vice president of marketing at eASIC. "Transistors in FPGAs are used for buffering, look-up tables, and switching, not just logic. That means that static-power leakage is immense," says Vasishta. "FPGAs leak like sieves, and a function in FPGA consumes 400 times more power than an equivalent function in standard cell."

"If you are pad-limited or need IP that is not available in FPGA, you might have to jump into a platform or cell-based ASIC regardless of volumes or complexity," says Yousef Khalilollahi, director of RapidChip marketing at LSI Logic.

Steven Kawamoto, senior marketing manager at NEC Electronics America Inc, says that design constraints offering high performance and low power sometimes force users to go directly to ASIC fabric and can't be adequately prototyped, even in FPGAs. "In these cases, structured ASIC allows users to prototype," says Kawamoto. "If you need low volume but the speed of an ASIC, you can move right away with structured ASICs."

FPGA vendors also offer volume breaks. Xilinx, for example, offers its EasyPath option to allow its users to mass produce FPGAs for 30% less in volume, starting at 3000 units by locking down a large portion of the design and cutting out test costs. "We don't create a new sil-

TABLE 1 STRUCTURED-ASIC ALTERNATIVES TO FPGAs AND CELL-BASED ASICs

Company	Structured-ASIC family	Designable layers	Total No. of layers	Designable gates (ASIC equivalent)	Process geometry and fab	Memory (bits)	Top speed (MHz)	Power (V)	Type of programming	Average NRE	Time from hand-off to silicon	Minimum unit volume	No. of structured-ASIC customers in 2004	No. of structured-ASIC customers as of May 5, 2005	Total structured-ASIC design starts in 2003	Total structured-ASIC design starts in 2004	Total structured-ASIC design starts in 2005
Altera	HardCopy II	Two layers of metal, three vias	NA	3.6 million	TSMC 90 and 130 nm	8.8M	350	1.2	None	$150,000	Eight to 10 weeks	1500	More than 20	More than 30	12	20	50
AMI Semiconductor	XPressArray XPA-1	Hybrid, five to seven	20 to 24	49,000 to 1.7 million	TSMC 0.18 micron through metal 2; metal 3 to 7 with AMIS 0.35 micron	38k to 1.4M DPRAM	200 system, 350 local	1.8	Metal mask	$50,000 to $100,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
	XPA-HD	Hybrid, five to seven	20 to 24	64,000 to 2.7 million	TSMC 0.18 micron through metal 2; metal 3 to 7 with AMIS 0.25 micron	38k to 1.4M DPRAM	200 system, 350 local	1.8	Metal mask	$50,000 to $100,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
	XPA-II	Hybrid, seven	25	511,000 to 4.9 million	TSMC 0.15 micron through metal 2, metal 3 to 7 with AMIS 0.25 micron	332k to 4.2M DPRAM (18-kbit blocks)	210 system, 500 local	1.5	Metal mask	$125,000 to $225,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
ChipX	CX3000	Two	Three	20,000 to 200,000	Charter 350 nm	352k	100	5/3.3 (I/O)	Metal mask	Less than $40,000	Five to six weeks	100	Claims 1600 designs since inception	NA	NA	NA	NA
	CX4000	Two	Five	20,000 to 550,000	UMC 250 nm	448k	125	2.5/3.3 (I/O)	Metal mask	Less than $50,000	Four to six weeks	100		NA	NA	NA	NA
	CX5000	Two	Six	25,000 to 1.1 million	UMC 180 nm	2.5M	200	1.8/2.5/3.3 (I/O)	Metal mask	Less than $100,000	Six to eight weeks	100		NA	NA	NA	NA
	CX6000	Four	Eight	100,000 to 1.5 million	UMC 130 nm	3.5M	300	1.2/1.8/2.5/ 3.3 (I/O)	Metal mask	Less than $225,000	Eight to 10 weeks	100		NA	NA	NA	NA
eASIC Corp	FlexASIC	One via layer, configured with one mask or by direct-write eBeam (zero masks)	Eight (eight metal/one poly)	3 million	STMicro, CMOS 130 nm	3M	250	1.2	Bit stream for logic plus direct-write eBeam or single photolithographic mask for routing	$0	Three weeks	No minimum	NA	NA	NA	NA	NA
Faraday Technology Corp	Netcomposer (NC-1) family (September 2005)	Four metal layers	One poly, eight metal, 42 layers	4 million raw gates, 2 million usable	0.13-micron UMC HS process	1M	Maximum CPU, 450; block, 300	1.2 (core), 3.3/5 (I/O)	Metal mask	$250,000	35 to 40 days	2000	NA	NA	NA	NA	NA
	Peripheral Composer (PC-1) family (August 2005)	Three metal layers	One poly, six metal, 32 layers	1 million raw gates, 500,000 usable	0.18-micron UMC G2 process	0.5M	Maximum CPU, 190; block, 100	1.8 (core), 3.3 (I/O)	Metal mask	$144,000	25 to 30 days	2000	NA	NA	NA	NA	NA
	PowerSaver Template (PST-1) family (December 2005)	Four metal layers	One poly, eight metal, 43 layers	4 million raw gates, 2 million usable	0.13-micron UMC HS process	1.5M	Maximum structured ASIC, 150	1.2 (core), 3.3/5 (I/O)	Metal mask	$200,000	35 to 40 days	2000	NA	NA	NA	NA	NA
Fujitsu	AccelArray	Three to five metal and via layers	Six metal	4 million maximum	Fujitsu 0.11-micron technology, 0.08-micron physical gate length	4.5M	311	1.2	Metal mask	$150,000	Four to eight weeks, depending on design	1000	NA	NA	NA	NA	NA
LSI Logic	RapidChip Platform ASIC	Four metal layers	NA	As many as 5.6 million usable ASIC gates	TSMC 110 nm and LSI Logic Gresham 110 nm	8M	More than 400, 20 levels of logic at 312	1.5, 1.8	Metal mask	$125,000	Eight to 10 weeks	1300	NA	NA	NA	NA	NA
NEC Electronics	ISSP1	Two	Seven	1.7 million	150 nm NEC	3.6M	200	1.5	Metal mask	$60,000 to $90,000	10 days	400	NA	NA	NA	NA	NA
	ISSP1-HSI	Two	Seven	1.7 million	150 nm NEC	3.6M	200	1.5	Metal mask	$80,000 to $100,000	10 days	400	NA	NA	NA	NA	NA
	ISSP-90	Two	Seven	6.5 million	90 nm NEC	5.6M	333	1	Metal mask	$150,000 to $190,000	Four to six weeks	400	NA	NA	NA	NA	NA
	CMOS12M (in July)	Five	Five to six	2.4 million	150 nm NEC	2.7M	200	1.5	Metal mask	$65,000 to $100,000	14 days	10,000	NA	NA	NA	NA	NA

icon product. We apply a new test methodology to the same product," says Patrick Dorsey, director of EasyPath and Configuration Solutions Division at Xilinx. "It is exactly the same silicon and the same product."

Because they are on the same silicon, the devices still have power and die-size limitations. Analysts say that until FPGAs vendors address those hard limitations, a market opportunity exists for structured devices.

WHY STRUCTURED?

"Structured ASIC is a product to solve a bunch of problems, and in this case, the problems are structural and not likely to go away," says Wawrzyniak. "Structured ASIC will only go away if someone figures a way to cut design time in half, cut NRE in half, and market windows widen greatly."

Wawrzyniak says that the structured-ASIC market was $200 million last year and predicts that it will grow to $1.5 billion by 2008.

> "IF YOU ARE LOOKING TO DEVELOP A CHIP THAT IS HIGH-COMPLEXITY BUT LOW-VOLUME, FPGA IS THE WAY TO GO."

Structured ASICs have a much lower NRE and volume requirement than traditional ASICs and a much faster turnaround time—anywhere from 10 days to 14 weeks (**Table 1**).

"The whole idea of platform ASIC is not just the savings in mask charges; three-fourths of the design is reused, and that can save you $5 million to $7 million in engineering effort," says Lewis. "You save on mask, but the bigger savings is on engineering."

Structured-ASIC customers typically need buy only one or two commercial-EDA tools—typically a synthesis tool from Synplicity, Magma, or Synopsys—spending $25,000 to $50,000. Some vendors follow the FPGA-vendor-tool model and offer customers OEM versions of design software for free.

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Jordan Selburn, ASIC and FPGA analyst with research firm iSuppli, says users are employing structured ASICs in a range of applications, so vendors are keeping busy creating slices, which are application-specific platform layers, to speed customers through tapeout and products to market.

"I don't know the exact number of slices LSI Logic has, but they are probably averaging one new slice per design," says Selburn, who predicts that the structured-ASIC market will reach $471 million by 2008, after posting what he estimates was revenue of $86 million in 2004.

GUIDELINES FOR CHOOSING

For high-complexity designs, analysts say, structured ASICs cost five to 10 times less in volume than equivalent-gate-count FPGAs.

Judging solely on volume, a consensus of semiconductor-industry analysts and vendors say that FPGA is likely the most viable fabric for high-complexity designs to 20,000 units, and structured ASIC is the most viable option from 100,000 to 3 million units. Above that number, traditional ASIC becomes more reasonable in volume.

"If you are looking to develop a chip that is high-complexity but low-volume, FPGA is the way to go," says Jerry Worchel, principal analyst, ASIC/ASSP and intellectual-property service at market-research company In-Stat. "If you need 1000 and 20,000 and the cost is within your budget constraints for the system, then an FPGA is a good way to go. You sure don't want to buy 100,000 FPGAs if they are $5 apiece, hence the structured-ASIC market."

"From 2000 units to around 250,000 units is where platform ASIC makes sense," says LSI's Khalilollahi. "Beyond that, cell-based ASIC makes more sense. As we move to finer process geometries, platform will make sense at higher volumes."

At what gate count structured makes more sense than FPGA and ASIC depends largely on who you ask.

Altera's Bismuth says that FPGA is the right option for low- to medium-density designs to 1 million gates, unless volumes are really high. Structured ASIC, he says, is ideal for designs of greater than a million gates. "For density above 5 million gates, there is nothing else available; you have to go to an ASIC," says Bismuth.

ASIC vendors, of course, believe the gate-count inflection point at which designers should consider structured ASIC over FPGA is much lower.

"If you have a small design around 50,000 FPGA gates, FPGAs are a good choice, because FPGA vendors have really come down in pricing," says Khalilollahi. "But when you really get to 250,000 to 500,000 ASIC gates, that's when the platform-ASIC proposition becomes valid."

Bismuth notes that security is another consideration. Structured devices, he contends, typically have better security and encryption features than do SRAM-based FPGAs. Of course, FPGA vendors, most notably Actel, have FPGAs with high-security features.

Manpower and skills are other considerations. Analysts point out that many design groups lack the employees or the experience to design a full-blown ASIC, but, they say, a designer with the skills to perform FPGA synthesis likely has enough knowledge to synthesize a structured device. EDN

You can reach Senior Editor Michael Santarini at 1-408-345-4424 and michaelsantarini@reedbusiness.com.

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Power Supply Control Solutions ... at the Touch of a Button

High Performance Analog Solutions from Linear Technology

Portable devices need to draw minimal current when off – ideally zero – to maximize battery life. Implementing push-button on/off control disconnects everything from the battery except the push-button control circuitry. Providing graceful power-up and power-down with minimal board space and minimal current draw is challenging, particularly when higher voltage battery packs are used. Linear Technology addresses the push-button interface challenge with a pair of tiny controllers.

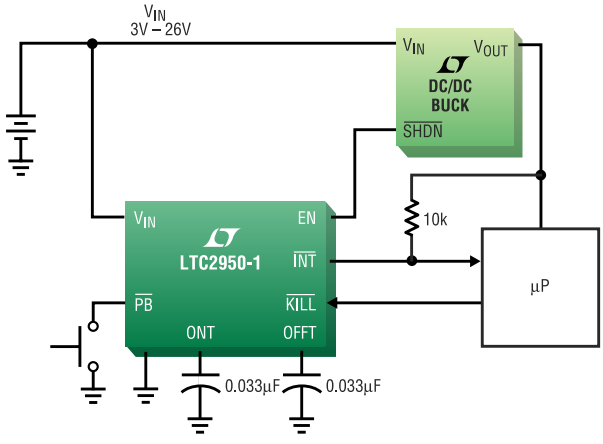

Figure 1. Push-Button Control of DC/DC Buck Converter

The LTC®2950 integrates a push button controller that provides enable control for DC/DC converters with processor interrupt logic and adjustable debounce timers. The part solves the inherent bounce problem associated with all mechanical contacts and operates over a 2.7V to 26V input voltage range to accommodate a wide variety of input power supplies. When powering off, the LTC2950 interrupts the system processor, alerting it to perform the necessary power down and housekeeping tasks. Once the system completes the power-down operations, it can command the LTC2950 to immediately disable power. The LTC2951 offers additional time for system power down, configured by an external capacitor. Offered in tiny 8-pin 2mm x 3mm DFN and TSOT-8 packages, the LTC2950 and LTC2951 save design time, as well as precious board space for portable instruments and handheld products.

Table 1. LTC2950/LTC2951 Feature Comparison

	LTC2950	LTC2951
Push-Button Control	✔	✔
Push-Button ESD Protection	10kV	10kV
ON debounce delay (Default)	32ms	128ms
Programmable ON time delay	✔	
OFF debounce delay (Default)	32ms	32ms
Programmable OFF time delay	✔	✔
System Shutdown delay (Default)	1024ms	128ms
Programmable KILL time delay		✔
Supply Current	6µA	6µA
Packages	2mm x 3mm DFN TSOT-8	2mm x 3mm DFN TSOT-8

High Voltage Operation at Low Current

Operating from 2.7V to 26V, the high-voltage design provides a unique advantage as a push-button debounce circuit. It connects directly to multi-battery stacks without the need for power-robbing resistors or level-shifting circuits. The input pin is rugged, too, providing 10kV ESD protection. But unlike most circuits in portable systems, the push-button interface must be active continuously

Power Supply Control Solutions ... at the Touch of a Button

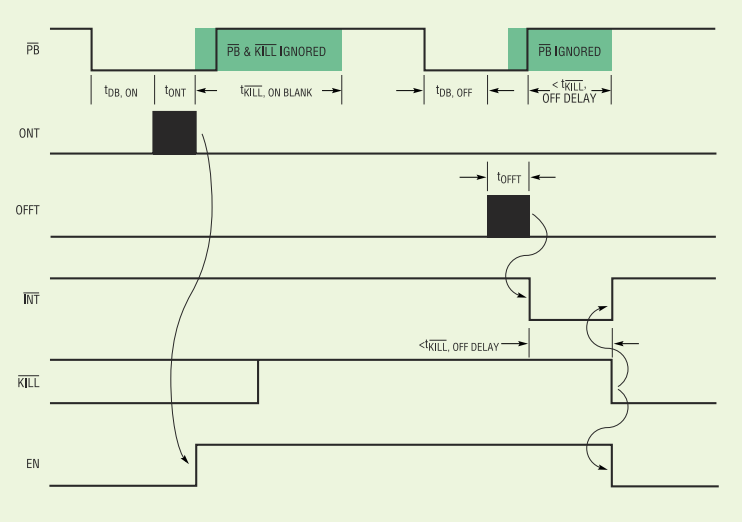

Figure 2. LTC2950 Timing Sequence

– there is no sleep mode or off state. The LTC2950 continuously monitors the push-button input for the next event, remembering whether the system is on or off. The supply current is low while monitoring, minimizing the drain on the battery.

System Interface

In addition to the debounce function, there is also a handshake function that works with the processor or system logic. There is an interrupt output and a kill input. During a "turn-on" event, the LTC2950 will disable power if the processor does not come back and release the kill input within a prescribed time. This ensures that the power-up occurs successfully. During the "turn-off" event, the LTC2950 interrupts the processor and warns that power will be turned off. It then waits for the processor to shut down and return a kill command before it disables the power, assuring complete and successful power-down. If no kill command comes back, perhaps due to the processor hanging up, power is turned off after 512ms.

Referring to the timing diagram in Figure 2, a transition on PB# initiates the power on sequence. The default delay is 32ms and the external ONT capacitor allows the user to configure longer delays. Once EN goes high, an internal 512ms blanking timer is started. This blanking timer is designed to give sufficient time for the DC/DC converter to reach its final voltage, and to allow the µP enough time to perform power on tasks. The $\overline{\text{KILL}}$ pin must be pulled high within 512ms of the EN pin going high. If not, the DC/DC converter will be disabled. The next transition on $\overline{\text{PB}}$ initiates the power off sequence. Similarly, the default delay is 32ms and the external OFFT capacitor allows the user to configure longer delays. At that point an interrupt is set, signifying that the DC/DC converter will be disabled in 1024ms. Once a system has finished performing its power down operations, it can set $\overline{\text{KILL}}$ low (and thus immediately shut off power), terminating the internal 1024ms timer.

Figure 1 shows EN controlling a DC/DC converter for the main supply to the system. The EN output is open drain; the LTC2950-1 is positive logic and the LTC2950-2 is negative logic. The $\overline{\text{INT}}$ and $\overline{\text{KILL}}$ signals communicate with the microprocessor.

The $\overline{\text{EN}}$ open drain output of the LTC2950-2 is designed for 10V so it can switch on/off an external P-channel power MOSFET. Figure 3 shows the LTC2950-2 ($\overline{\text{EN}}$) switching an external MOSFET for power path control in a two cell Li-Ion battery application. This allows a user to

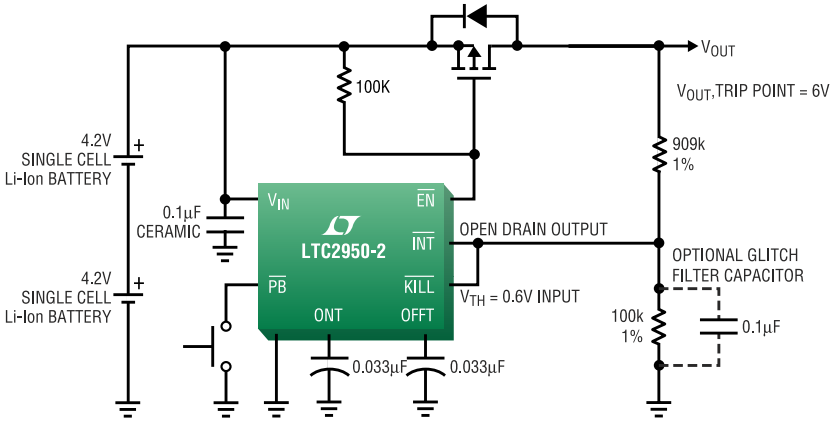

Figure 3. Push-Button Control of P-Channel MOSFET for Power Path Control

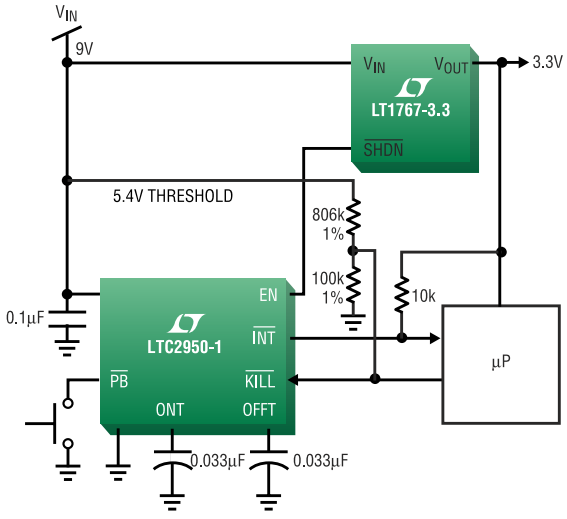

Figure 4. Push-Button Control of LDO with Low Battery Monitor

connect/disconnect a power supply or back-up battery to its load by toggling the $\overline{PB}$ pin. The $\overline{INT}$ and $\overline{KILL}$ pins are connected to the output of the MOSFET through a resistive divider. Therefore, $\overline{KILL}$ will be pulled low when $\overline{INT}$ goes low, killing power immediately. The $\overline{KILL}$ pin also serves as a voltage monitor. When V_{OUT} drops below 6V, the $\overline{EN}$ pin is brought high 30µs later.

As in the previous circuit, the circuit in Figure 4 takes advantage of the precision analog comparator used for the $\overline{KILL}$ input so it can be used as a voltage monitor. It is driven by a low leakage open drain output of the µP. It is also connected to a resistive divider that monitors the battery voltage (V_{IN}). When the battery voltage falls below 5.4V, the voltage at the $\overline{KILL}$ pin falls below 0.6V and the EN pin is quickly pulled low. The DC/DC converter shown has an internal pull-up current on its $\overline{SHDN}$ pin; thus a pull-up resistor on EN is not needed.

The LTC2951 is identical to the LTC2950 except that it trades the adjustable ON timer for an adjustable $\overline{KILL}$ timer. Figure 5 shows the same circuit as in Figure 1 except that the ON debounce time is fixed at 128ms internally and the external capacitor connected to the KILLT pin extends the time allowed for the processor to complete its shutdown sequence and release the $\overline{KILL}$ pin from the default 128ms to 339ms, as shown in Figure 5.

Power path control between a battery and a wall adaptor is shown in Figure 6. The LTC4413 is a two-channel ideal diode designed to reduce heat, voltage drop and board space as well as preserve battery life. The device is ideal for applications requiring an ideal diode OR function for load sharing or automatic switchover between two input power sources. The LTC4413 has control access to each ideal diode but in this circuit the $\overline{EN}$ output from the LTC2950 is tied to each of the inputs, activating both channels at the same time. $\overline{INT}$ and $\overline{KILL}$ are tied together, simplifying the power-up/down sequence when a processor handshake is not required.

Push-button control is not just for battery-powered systems. Large systems with multiple supplies and demanding sequencing requirements can benefit from simplified on/off control. Figure 7 shows the LTC2950 controlling a P-channel MOSFET in series with four supplies that are sequenced by the LTC2924. When power is enabled, the ON pin of the LTC2924 is pulled high to begin the power-up sequence. Each output is monitored and the $\overline{DONE}$ output signals that the power-up sequence is successfully completed. This releases the $\overline{KILL}$ input of the LTC2950. When the push-button commands the system to power down, the $\overline{INT}$ pin pulls the ON pin of

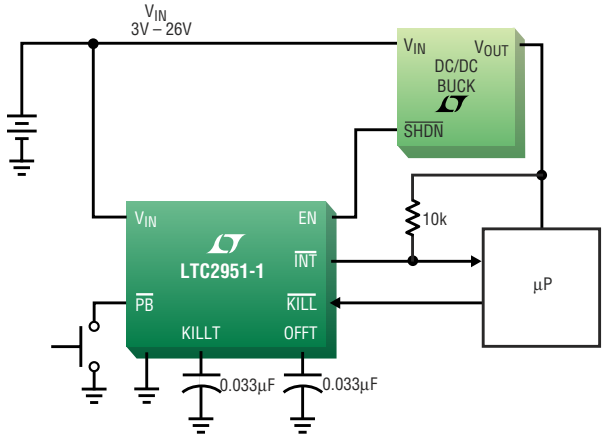

Figure 5. Push-Button Control with Extended Processor Shutdown Time

Power Supply Control Solutions ... at the Touch of a Button

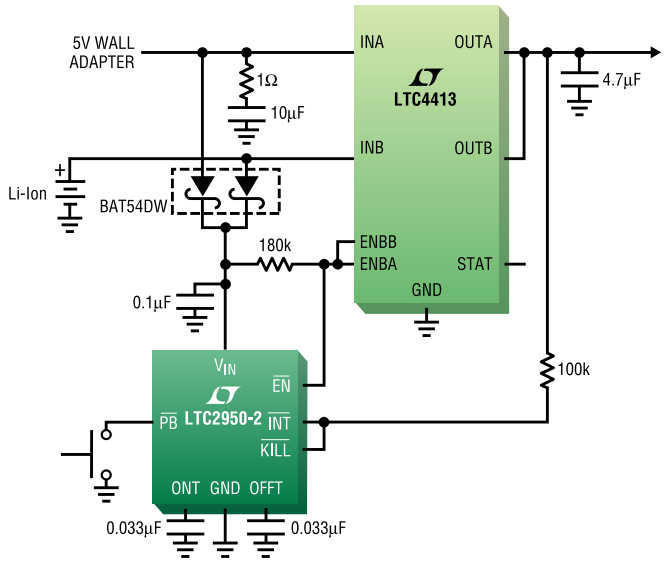

Figure 6. Push-Button Control of a Dual Ideal-Diode for Power Path Control

the LTC2924 low to begin the power-down sequence. The $\overline{\text{DONE}}$ pin drives $\overline{\text{KILL}}$ low when all supplies have successfully powered down and the LTC2950 disconnects power using the P-channel MOSFET.

Portable and non-portable devices utilize push-button control to enable and disable power. Often this requires a tiny, low current solution that is capable of operating from high input voltages. The LTC2950 and LTC2951 provide this solution and also interface with the processor to assure proper execution of power-up and power-down routines. In the tiny 2mm x 3mm DFN package with just a few optional external components, these devices offer simple and secure push-button control.

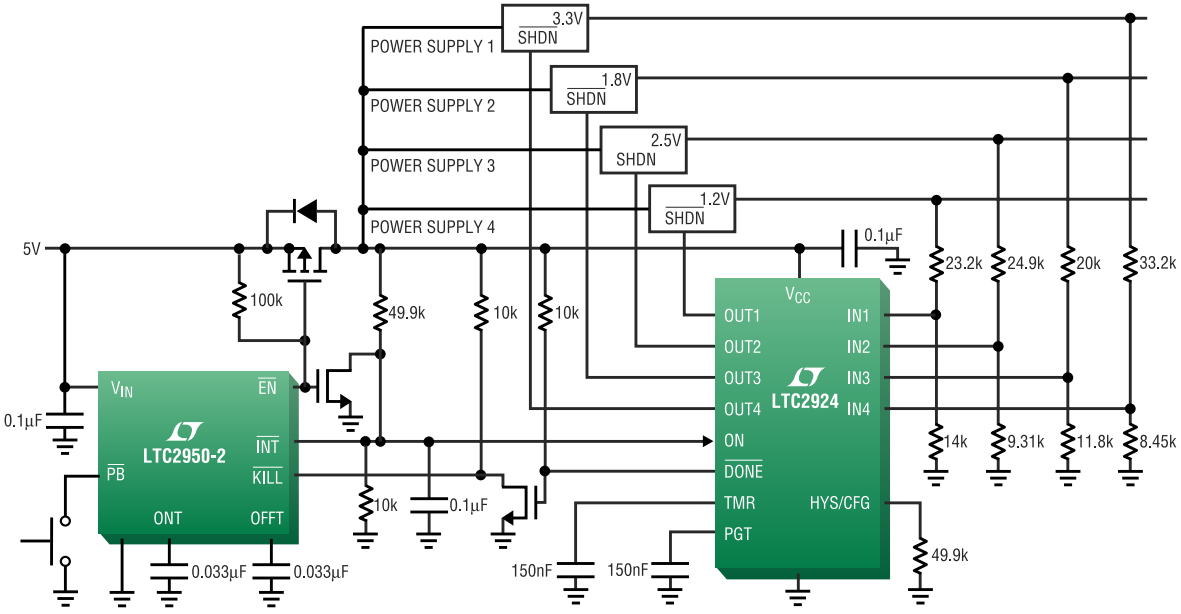

Figure 7. Push-Button Control of On/Off Power Supply Sequencing

BY DONALD W CORSON • EM MICROELECTRONIC

Windowed-watchdog timers enhance system security

A SUPERVISORY FUNCTION ENABLES SYSTEM RECOVERY TO PREVENT EXECUTION ERRORS.

As microprocessor-controlled systems begin to carry out more and more functions involving human safety, the importance of close performance monitoring is increasing. The low cost and range of features for many of today's microprocessor functions allow their use in many applications that were previously the domain of dedicated hardware. Although microprocessors are highly flexible tools, the probability of code errors in their programs lowers their functional reliability. Defensive programming techniques, such as filling unused ROM with halt or illegal instructions to trap illegal jumps in code space, will aid in program debugging. They can also provide a small but useful mechanism for gracious recovery when deployed. But even with the most careful and complete testing, you won't find every error; no method can ensure 100% coverage.

Systems that could cause bodily injury if they malfunction require high reliability. Examples of such systems include automotive antilock-braking or steering systems; medical instruments, such as insulin pumps; robots; industrial-control systems; automatic doors; nuclear-power-plant controls; and avionics. These systems must be able to recover from a crash without human assistance, such as someone pressing a reset button, because such intervention would probably occur too late to prevent injury.

A watchdog timer is a subsystem that can cause a program reset or NMI (nonmaskable interrupt) if a microprocessor does not react within a certain amount of time. In many cases, the timer can catch a misbehaving microprocessor system. For highly sensitive applications, designers should use windowed-watchdog timers, which activate when system code clears them either too slowly or too quickly. Their use adds another class of recognizable program errors or faulty hardware behavior. Ideally, a watchdog-monitored system can restart itself back into a working state without the user even knowing that an error occurred. To achieve this level of comfort, the system and software design must be able to accept a reset at any time and resume normal operation without operator intervention.

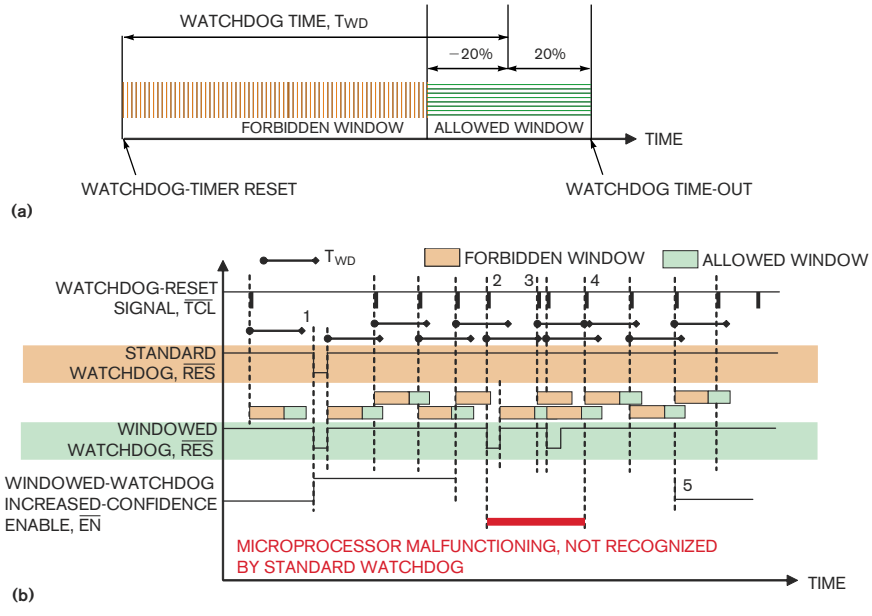

Figure 1 Two distinct periods exist in the timing of a windowed-watchdog timer (a). Comparing windowed-watchdog timers and standard-watchdog timers reveals the effect of the windowing period (b).

Many microcontrollers offer an internal programmable watchdog with similar functions. Software can disable these internal watchdog timers, so they do not provide the same protection for safety-critical applications as do independent external watchdog circuits. Critical applications should employ an external watchdog-reset circuit.

BASIC OPERATION

Standard watchdogs are incrementing counters that set their output when the counters reach their maximum value. The microcontroller must reset the counter by creating a falling edge on the timer's clear input. If the program execution is faulty because of a program error, or if an external disturbance slows the program execution, the counter will reach its maximum value, and the

watchdog-timer output will activate. This approach catches problems such as code executing ("hanging") in endless loops. It does not, however, trigger for errors such as routines that return before their normal-completion cycle, causing the program execution to be faster than expected.

For highest security, a windowed watchdog demands that the timer's clear-input edge be within a certain window. If the signal arrives before or after this timing window, it triggers the output signal to either reset the processor or activate other error handling. This type of watchdog effectively covers programs that execute both too slowly and too quickly.

Not all errors are due to software bugs or conventional processor or circuitry problems. Another cause of error is when the crystals in clock and resonance circuits jump to spurious modes because of external shocks. Although in this situation, the crystal will probably return to its proper frequency after a short time, the processor may be in danger of improper program execution. The windowed watchdog can catch this behavior.

In **Figure 1a**, the watchdog timing of a windowed-watchdog timer divides into two periods. The time when the falling edge of the $\overline{TCL}$ input signal or WDI (watchdog-input) signals an error is called the forbidden window. The allowed window is the time when the $\overline{TCL}$ input's falling edge resets the timer and is accepted. (Some documentation refers to the allowed window as the open window and the forbidden window as the closed window.) The time after the allowed window is a timeout. In general, windowed-watchdog products allow programming the watchdog time, T_{WD}, using an external resistor or capacitor.

As an example, for the EM6150/51, the allowed window is ±20% of the T_{WD}. The forbidden window is the time up to 80% of T_{WD}. The watchdog timeout is at T_{WD}+20%. If no $\overline{TCL}$ has been received until the end of the allowed window, the watchdog immediately produces a reset pulse. Both a falling flank on $\overline{TCL}$ during the forbidden window and a timeout after T_{WD}+20% asserts reset and removes the enable. Note that the timing for the next period starts immediately after the falling edge of $\overline{TCL}$.

To understand the benefits of using a windowed-watchdog timer over a standard watchdog timer for high-reliability operations, consider the five following events (**Figure 1b**):

1. reset after watchdog timeout;
2. reset caused by $\overline{TCL}$ arriving too soon, during forbidden window;
3. timing OK;
4. reset caused by $\overline{TCL}$ arriving too soon, during forbidden window; and
5. enable asserted after three good $\overline{TCL}$ inputs.

The events represent the following activities: At Event 1, both the standard-watchdog timer and the windowed-watchdog timer generate a reset, because the T_{WD} period passes without a signal on the $\overline{TCL}$ input. Next, three correct watchdog cycles cause assertion of the increased-confidence enable output. At Event 2, the $\overline{TCL}$ signal arrives too early, during the forbidden window in the windowed-watchdog timer. Therefore, the system immediately asserts the $\overline{RES}$ output and revokes the $\overline{EN}$ output. At Event 3, the timing is OK, but at Event 4, the $\overline{TCL}$ signal again falls within the forbidden window of windowed-watchdog timer, causing another reset. In each case, the watchdog timing begins at the falling edge of the last $\overline{TCL}$ input. Note that in events 2 and 4, a standard-watchdog timer does not detect that the processor is malfunctioning and working too fast, whereas a windowed-watchdog timer does. Note also that the $\overline{EN}$ output has not yet been asserted. At Event 5, the system again stabilizes itself and asserts the increased-confidence enable $\overline{EN}$ after three good watchdog cycles.

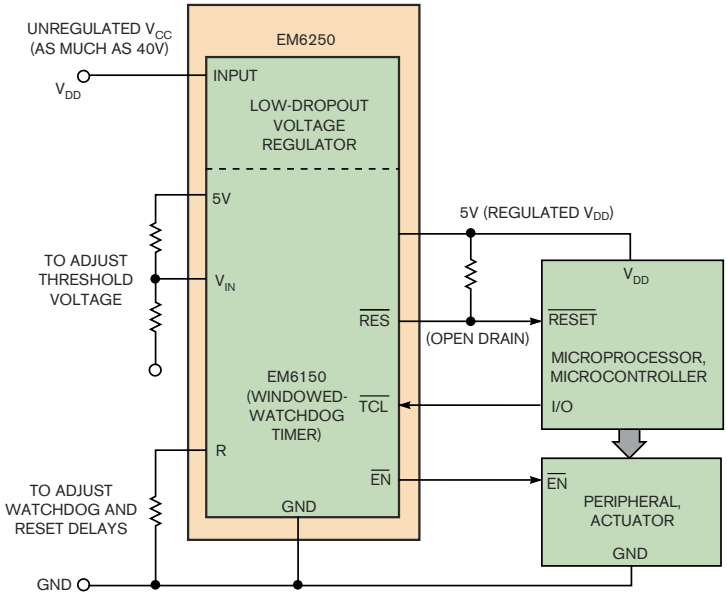

Figure 2 Some watchdog timers, whether windowed or standard, also incorporate an LDO, which makes for an especially useful component in highly decentralized systems.

Windowed-watchdog circuits generally also include all of the features of a standard voltage-reset circuit, such as a timeout-reset period or threshold voltage. You can either factory-preprogram these elements or set them using external components, allowing for increased flexibility.

Distributed systems are other applications in which windowed watchdogs help maintain total system confidence. In systems in which a master provides timing or synchronization messages to the slave processors, a standard watchdog can detect a missing master unit, or a master unit that is failing in a slow direction ("failing slow"). A windowed watchdog increases the error coverage to include multiple conflicting masters on the bus, or masters that are failing in the fast direction ("failing fast").

For applications that could cause human injury, such as automatic car windows or doors, it is a good idea to use a windowed watchdog, which is today's state of the art in design. To increase security in applications driving motors or actuators, designers can use an increased-confidence enable-output func-

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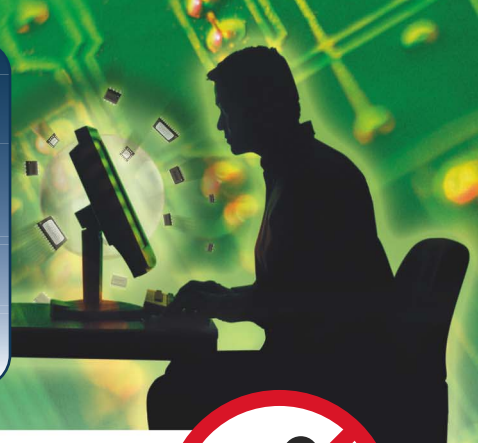

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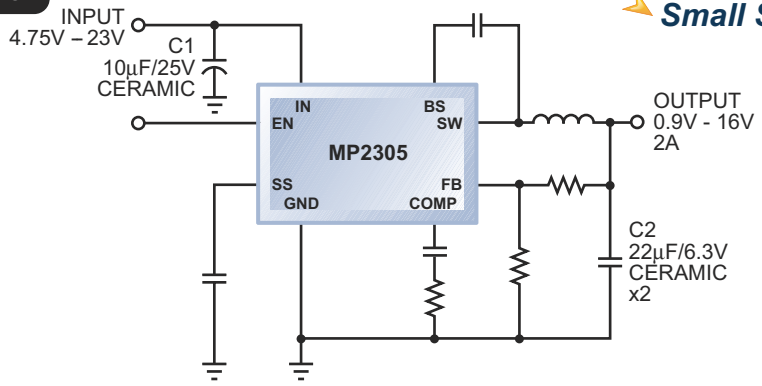

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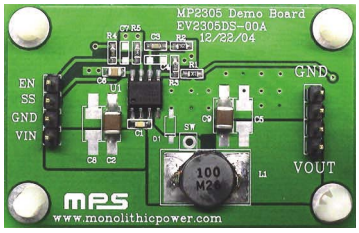

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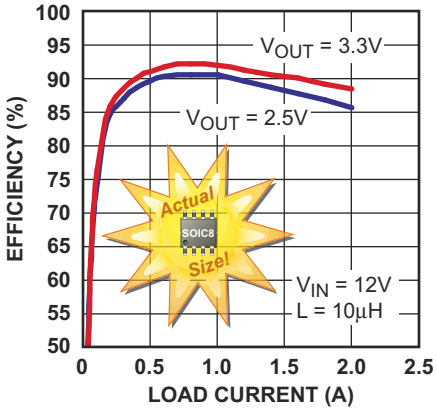
Featured Synchronous Bucks				
Part	Frequency	V_{IN} (V)	I_{OUT} (A)	Package
MP2104	1.7MHz	2.5 - 6	0.6	TSOT23-5
MP2109*	1.0MHz	2.5 - 6	2x 0.8	QFN10 (3x3)
MP2106	800kHz	2.6 - 13.5	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2	SOIC8
MP1570	340kHz	4.75 - 23	3	SOIC8
Featured Non-Synchronous Bucks				
MP2361	1.4MHz	4.75 - 23	2	QFN10 (3x3)
MP2364*	1.4MHz	4.75 - 23	2x 1.5	TSSOP20
MP2354	380kHz	4.75 - 23	2	SOIC8
MP1593	385kHz	4.75 - 28	3	SOIC8

** Dual Output*

MP2305
Efficiency vs Load Current



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tion for gating motor signals. For instance, this function can immediately stop the motor movement when a system cannot trust the processor behavior and allow it again only when it is confident that the processor is running properly. The watchdog timer reasserts this signal only after it sees three good $\overline{TCL}$ edges and removes the signal simultaneously with the $\overline{RES}$ output assertion when it detects a processor malfunction.

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SOFTWARE CONSIDERATIONS HAVE A ROLE

Adding a windowed watchdog to a system is an important step in increasing system confidence, but if the watchdog timer's service routine is a timer-triggered interrupt routine just for this watchdog, it is useless. It is very possible that the entire system could crash, yet the timer-triggered interrupt continues to service the watchdog at the appropriate intervals, indicating that all is well.

Always keep in mind the basic rules of embedded programming. Always fill unused program memory with defined patterns and be sure that this pattern is defined for every possible address in memory where a misguided jump could land. The strategy depends on the processor. You can use multibyte or word instructions where a wayward jump could land in the middle of an address boundary.

In general, use halt instructions or known illegal instructions if the processor core traps them, as either instruction traps illegal jumps regardless of the cause. The halt causes a watchdog to trigger, whereas the trapping and processing action that occurs after an illegal instruction depends on the system architecture. Both techniques are useful in a debugging environment to help trace the cause of the illegal jump. In production units, you can use them to set a reset or to trigger a routine that puts the equipment in a known or safe mode.

NEVER SERVICE A WATCHDOG TIMER USING A ROUTINE SOLELY FOR THAT PURPOSE.

Never service a watchdog timer using a routine solely for that purpose. The only exception to this rule could be in multitasking systems. Because such systems are often nondeterministic, one option for periodically servicing the watchdog timer is to have a monitor task that services the watchdog, depending on clues that other tasks leave. By incrementing counters when they have finished certain processing functions, for example, the system tasks can leave enough information for a monitoring task to decide whether the system is well. Because this approach uses software to take over a hardware-safety function, designers should make sure the system is sufficiently deterministic so that the watchdog-timer service function uses a working routine.

Also include reset-time processor validation in the embedded-system design. Although processor failures are rare and most often catastrophic, partial failures do occur. Processor validation, which you must do in assembly-language code, should begin with a simple unconditional jump command and then continue to all of the commands that the application uses, where the tested commands can find use later in the tests for other commands. Although programmers may not like creating such test code, it can provide considerable system security and even cost savings, because it allows the system to demonstrate that the processor is thoroughly tested, both in production test (possibly eliminating the need for a dedicated testing station) and in application use.

DON'T FORGET THERMAL CONSIDERATIONS

Windowed-watchdog-timer circuits are also available with one built-in LDO (low-dropout regulator) or more on chip. Such circuits are especially useful in decentralized systems, such as automotive and industrial-automation applications, as they can monitor the security and provide the power-supply regulation in one component (**Figure 2**).

As with any voltage regulator, the pc-board layout is important to the success of the design. The routing of the decoupling capacitors to the supply and ground traces or planes must be clean and short. Circuitous paths increase the circuit inductance and possibly the cross-coupling between inputs and outputs. Clean separation between the logic supply and the power portion of the circuitry is especially important in circuits controlling electrical motors, due to the large spikes that they produce on the power-supply lines.

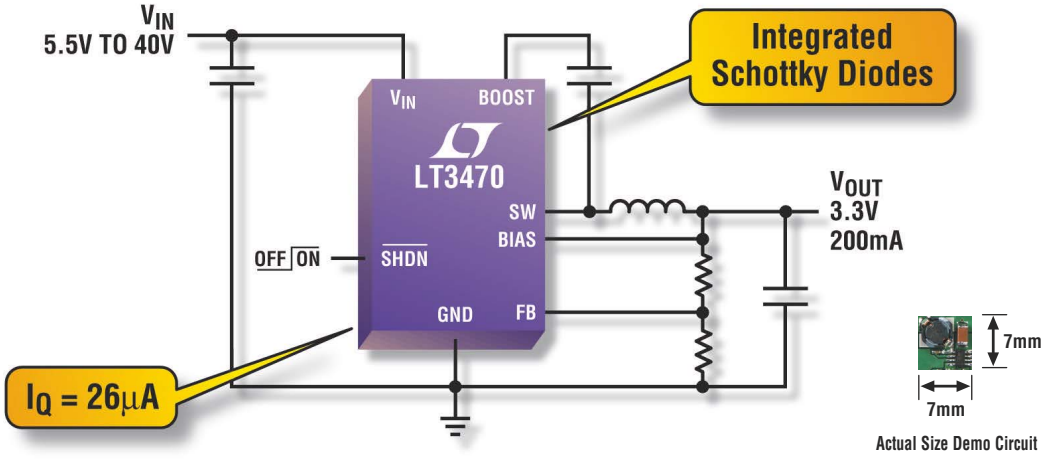
Also, designers should take into account thermal issues when planning the layout. The housing of many ICs containing LDOs has a heat-sink contact called a "thermal slug" that you must solder to the pc board. The pc board should provide adequate surface area so it can function as a radiator around the chip. It is best on both board sides to have circuit planes that connect to the slug using thermal vias, to transfer the heat from the chip as efficiently as possible. The actual thermal resistance in any application depends greatly on the physical configuration of the complete module, pc-board cooling surfaces, thickness, airflow, convection, horizontal or vertical orientation, and other factors.

Watchdog components that can recognize that they are being placed in sleep mode, and so adapt their behavior to reduce system power consumption without decreasing security, are also available. These components suit ultralow-power applications using sleep mode, such as those for CAN-bus communication, in which you can disable functional units under software control. EDN

AUTHOR'S BIOGRAPHY

Don Corson began his career in computer-peripheral development at Philips in Germany. For the last five years, he has been with Swatch Group and EM Microelectronic. Corson was responsible for the battery system for Swatch's hybrid-car project and works at Swatch Group's semiconductor fab and design company, EM Microelectronic, on battery-related low-power, low-voltage projects. You can reach him at dcorson@emmicroelectronic.com.

40V_{IN}, 200mA Out in a ThinSOT



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LT1616	600mA	3.6V to 25V	1.4MHz	Single	1.9mA	ThinSOT
LT1933	750mA	3.6V to 36V	500kHz	Single	1.6mA	ThinSOT
LT1936	1.9A	3.6V to 36V	500kHz	Single	1.8mA	MSOP-8
LT1940	1.8A x 2	3.6V to 25V	1.1MHz	Dual	3.8mA	TSSOP-16

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READERS SOLVE DESIGN PROBLEMS

Contact-debouncing algorithm emulates Schmitt trigger

Elio Mazzocca, Technical Consultant, Adelaide, South Australia

Among other interface problems, contact bounce complicates the connection of mechanical contacts or any noisy digital input signal to a microcontroller. Although designers have proposed a variety of hardware and software approaches that address the problems that contact bounce poses, no one has yet claimed a definitive and predictably stable approach. (For a sampling of approaches, see **references 1** through **10**.) The usual hardware approach to eliminating contact bounce comprises an RC filter followed by a Schmitt trigger (**Figure 1**). You can extend the filter's effectiveness simply by increasing the RC time constant at the expense of increased response time.

Software-debouncing methods usually include 1-bit processing, which involves twice reading the contact's input state with a fixed delay between the two readings. You can also implement a state machine or launch an input signal through a shift register and wait for three or four register-output states that haven't changed. The low efficacy of 1-bit processing approaches stems from designers' erroneous assumptions that seemingly simple debouncing tasks can tolerate equally simple software. However, a detailed study of many types of contacts reveals a range of complex and sometimes unexpected behaviors. This Design Idea documents a more comprehensive method that can easily handle all mechanical contact interfacing to microcomputers.

The debouncing method applies full 8-bit-processing and digital-filtering techniques to digital inputs. Using as few as 20 assembly-language instructions that execute in 19 machine cycles on an ATmega8 microcontroller, the method produces a robust debouncing action (see **Listing 1** at the Web version of this Design Idea at www.edn.com/edn050707di1).

The software closely simulates the hardware circuit in **Figure 1** by using a first-order, recursive, digital lowpass filter followed by a software Schmitt trigger. In contrast to 1-bit software debouncers that generally do not apply processing to inputs, this debouncing algorithm is effective because it "remembers" past input transitions and assigns a "weight" to each transition depending on how long ago it occurred. Furthermore, you can alter the filter's settings on the fly to meet changing conditions by modifying its thresholds and hence its execution time, or time constant, from the main program. The basic recursion algorithm comprises present output value=(¼)×input value+(¾)×previous output value, or, $Y_{NEW}=(1/4)\times X_{NEW}+(3/4)\times Y_{OLD}$.

To avoid register overflow and instability, the value of Y_{OLD} and X_{NEW} must be less than 1, which for an 8-bit microprocessor translates to values of less than 256 for X_{NEW} and Y_{OLD}. Consequently, the input $(1/4\times X_{NEW})$ to the filter is either 0 or 63. You then apply the output value, Y_{NEW}, to the software Schmitt trigger. The trigger uses the following algorithm: If Y_{NEW}>hi, and flag=0, then flag=1, and out=1. If (Y_{NEW}<lo, and flag=1, then flag=0, and out=0.

Hardware Schmitt triggers typically have fixed thresholds of one-third and two-thirds of the power-supply voltage. However, the software allows widening these thresholds and thus increasing the filter's time constant. In operation, a timer-interrupt routine should execute the debouncing program every 4 to 5 msec. Becausee one time constant equals the period of one interrupt, using thresholds of 15 and 240 causes the routine's output to "trigger" after 11 interrupts, or 44 to 55 msec, which ade-

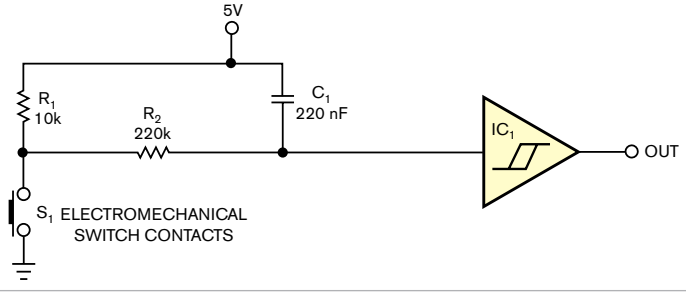

Figure 1 A basic switch-contact debouncer consists of an RC network followed by a Schmitt-trigger circuit.

DIs Inside

quately processes most switches' contact bounce.

You can easily modify the main filter coefficient to provide different filtering-time constants. For particularly troublesome contact bounce, you can use the following recursion formula, which requires 16 time constants to trigger the software Schmitt routine. $Y_{NEW}=(1/16)\times X_{NEW}+(15/16)\times Y_{OLD}$. You can implement this algorithm with only eight assembly-language instructions, whereas the Schmitt-trigger routine requires 12 instructions. When you combine both of these routines, the software Schmitt trigger updates bit 0 of a register, which the main program loop should continuously check to ascertain the contact's status. As an alternative, you can activate a software interrupt to signal a contact's status change. To do so in the AVR architecture, you write to that port bit that functions as an external interrupt input.

Always avoid connection of mechanical contacts to interrupt inputs unless the contacts undergo hardware debouncing. Otherwise, the contacts may bounce dozens of times, unnecessarily consuming processor-machine cycles. The software routine reads the inputs only every 4 msec and thus imposes additional filtering on the inputs. Simulation and practical testing have confirmed that the debouncing algorithm behaves as expected, producing clean output transitions when enduring noisy contacts. When you program the assembly-language source code accompanying this Design Idea into an Atmel Atmega8, the code turns on an output LED connected to Port_B bit 0 when Port_D bit 0 of the microcontroller goes to ground.

A simulated input waveform (pind0) and its corresponding output log file (portb0.log, both available at the Web version of this Design Idea at www.edn.com/050707di1,) illustrate the filter's excellent debouncing capabilities. Beginning with a key closure at 10 msec, the stimulus loads into the AVR Studio integrated development environment. After multiple input transitions, the output-log file shows a single output transition occurring at 55.333 msec. The software effectively filters out the three input pulses starting at 56.1 msec (**figures 2** and **3**).EDN

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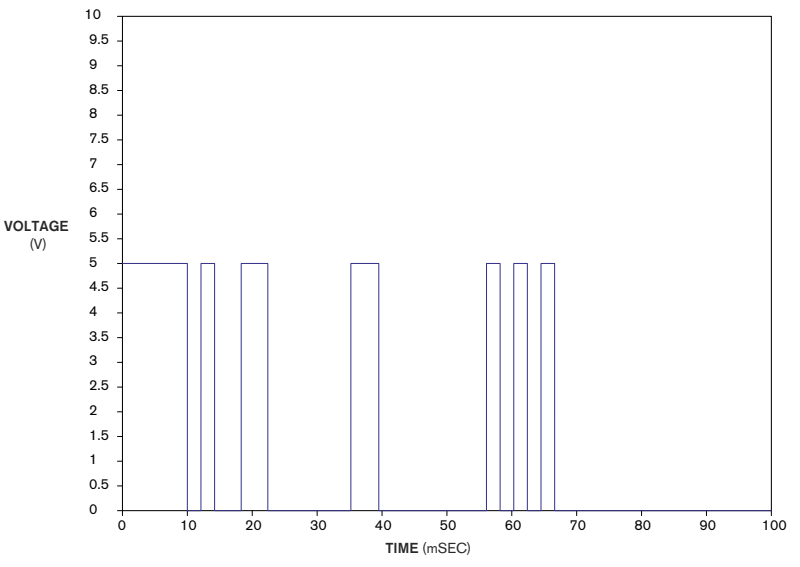


Figure 2 Switch contacts first close at 10 msec and then bounce erratically for more than 50 msec before reaching a stable closed condition.

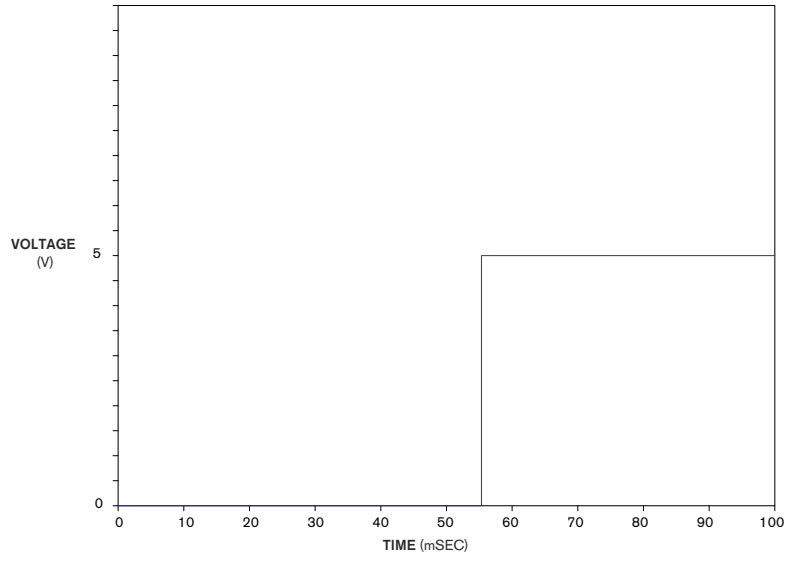
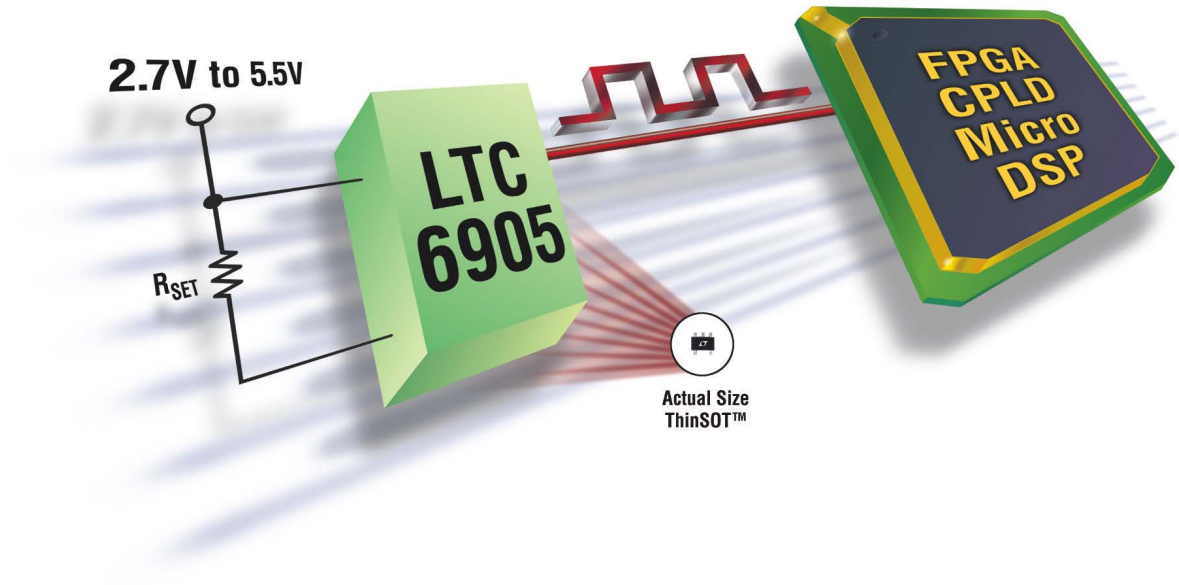


Figure 3 The debouncing-software routine signals that the contacts have closed only after bouncing ceases.

170MHz Clock in ThinSOT



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LTC6903	SPI Port	68MHz	3.1mA	MSOP-8	0.1% Resolution, 10ppm/°C Drift
LTC6904	I^2C Port	68MHz	3.1mA	MSOP-8	0.1% Resolution, 10ppm/°C Drift
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Inexpensive peak detector requires few components

Anthony H Smith, Scitech, Bedfordshire, England

Requiring no rectifier diodes, the positive peak-detector circuits in **figures 1** and **2** exploit the open-drain output of a Texas Instruments TLC372 fast comparator, IC_1. Both versions of the detector are simple and inexpensive and provide a buffered, low-impedance output at V_{OUT}. In addition, the TLC372's high typical input impedance of $10^{12}\Omega$ eliminates any need for an input buffer stage. As **Figure 1** shows, the detector's output voltage at the output of op amp IC_{2A} applies a feedback signal for the comparator and acts as a reference level for comparison with the input signal's amplitude. Upon first application of input signal V_{IN}, the voltage on the hold capacitor, C_1, is 0V, and V_{OUT} is also 0V.

When the input signal goes more positive than the output voltage, the comparator's internal output MOSFET turns on and sinks current through R_1. Provided that R_2 is relatively large, charging current flows into C_1 from IC_{2A}'s output. Over several cycles of the input signal, the charge on C_1 builds up, and V_{OUT} rises to the point at which it slightly exceeds the peak level of V_{IN}. For as long as V_{OUT} is slightly greater than V_{IN}, IC_1's output MOSFET remains off, and C_1 receives no additional packets of charge.

As a consequence, the charge stored on C_1 starts to dissipate as the capacitor discharges through R_2 and through the bias-current path into IC_{2A}'s inverting input. V_{OUT} gradually falls until it is just below the peak level of V_{IN}. The next positive peak of V_{IN} trips comparator IC_1, which pulls current through R_1, "topping up" the charge on C_1. This process produces a dc level at V_{OUT} that closely approximates the positive peak level of the input waveform. The values of R_1, R_2, and C_1 determine the ripple voltage present on V_{OUT}.

IC_{2A}'s inverting input is held at virtual ground potential, so whenever IC_1's output MOSFET turns on, the voltage across R_1 approximately equals the negative-supply-rail voltage, $-V_S$. Therefore, using a small value of R_1 injects a relatively large pulse of current into C_1, thus allowing the circuit to respond quickly to a sudden increase in input-signal amplitude—that is, a "fast-attack" response. However, if the value of R_1 is too small, the positive-going ripple on V_{OUT} becomes excessive and can lead to bursts of oscillation around peak values of V_{IN}.

For a given value of R_2, the value of C_1 determines the circuit's "delay time."

(continued on pg 92)

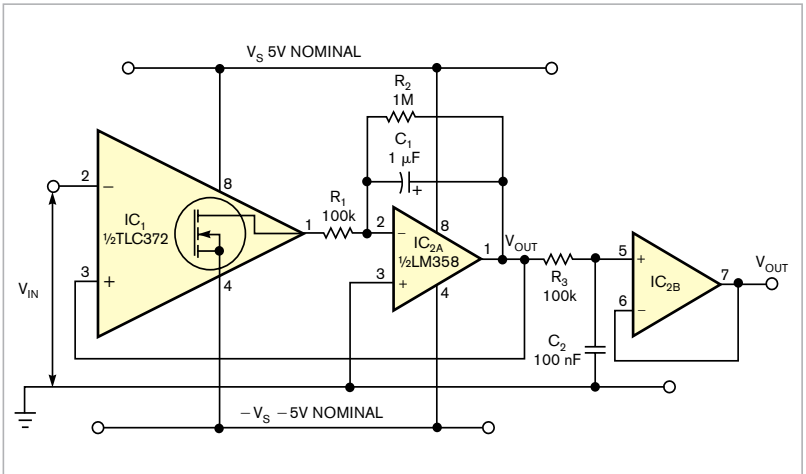

Figure 1 The dual-power-supply-voltage version of this positive peak detector requires only two active devices: a comparator and a dual operational amplifier.

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DESIGN NOTES

Low Distortion, Low Noise Differential Amplifier Drives High Speed ADCs in Demanding Communications Transceivers

Design Note 366

Cheng-Wei Pei

Introduction

Today's communications transceivers operate at much higher frequencies and wider bandwidths than those of the past. Combining this with higher resolution requirements, transceiver design can become daunting. For engineers designing these systems, small noise and distortion budgets leave little flexibility when choosing system components.

The LT®1993-x is designed to meet the demanding requirements of communications transceiver applications. It can be used as a differential ADC driver or as a general-purpose differential gain block. For single-ended systems, the LT1993-x can replace a transformer in performing single-ended to differential conversion without sacrificing noise or distortion performance.

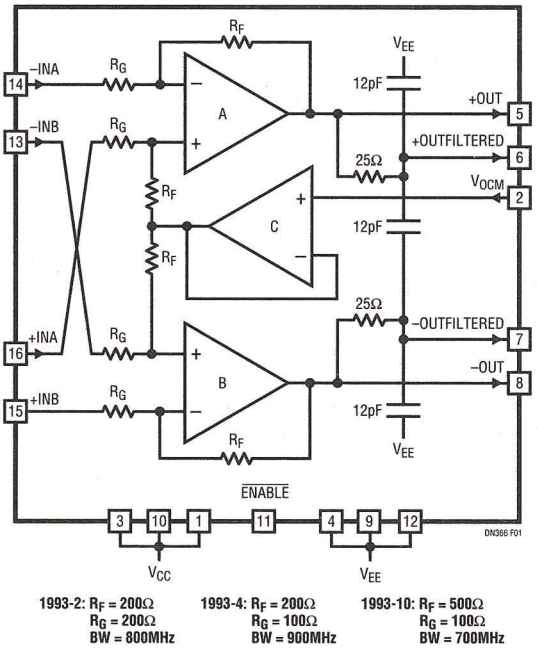

Figure 1. Block Diagram of the LT1993-x and the Differences Between the Gain Options. Input Impedance Is 200Ω for the 6dB Version and 100Ω for the Other Two Versions

LT1993-x Features

The LT1993-x is a fully differential input and output amplifier with up to 7GHz of gain-bandwidth product and an impressive feature set. There are three fixed-gain options with internal matched resistors: gain of 2 (6dB), gain of 4 (12dB) and gain of 10 (20dB). The LT1993-x is DC-coupled, precluding the need for DC blocking capacitors on the inputs and outputs. The output common mode voltage is independently controlled with an external pin, allowing optimal bias conditions for the ADC inputs. The LT1993-x features two sets of differential outputs: a normal output and a filtered output. The output filter eliminates additional filtering in many applications, but if necessary, additional filtering can be achieved with a few external components. Figure 1 shows a block diagram of the LT1993-x.

High Speed ADC Driving

One of the more challenging tasks in a modern communications transceiver is driving the analog-to-digital converter (ADC). Today's converters sample data at tens to hundreds of Megahertz with up to 16 bits of resolution. With each sample cycle, the switching of the internal ADC sample and hold injects charge into the output of the driver which must absorb the charge and settle its output before the next sample is taken. This charge injection is inherent in nearly all high speed, high resolution ADC topologies and must be considered when choosing a suitable driver.

The LT1993-x was designed specifically to drive high speed ADCs to their full potential. With a 3.8nV/$\sqrt{\text{Hz}}$ voltage noise specification and –70dBc of harmonic distortion at 70MHz ($2V_{P-P}$ differential output), the LT1993-x meets and exceeds the requirements for driving high resolution high speed ADCs. Figure 2 shows an FFT of sampled data taken on a 70MHz input signal with the LT1993-2 driving an LTC®2249 sampling at 80Msps.

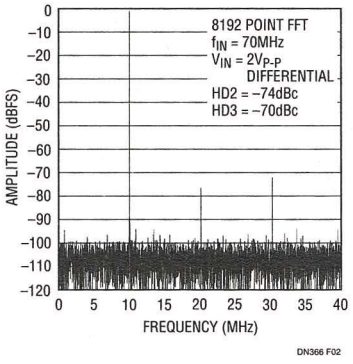

Figure 2. FFT Data Taken Using the LT1993-2 and the LTC2249 ADC Sampling at 80Msps. The Second Harmonic Is at –74dBc and the Third Harmonic Is at –70dBc

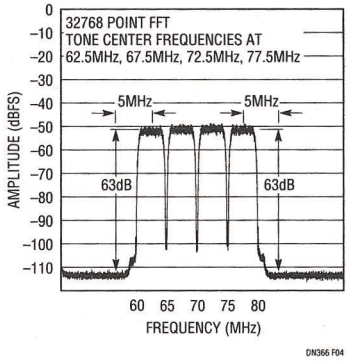

Figure 4. FFT Data Taken from the Output of the LTC2255 ADC. The Low IMD of the LT1993-2 Preserves the Signal-to-Noise Ratio of the WCDMA Channels

WCDMA Amplifier and ADC Driver

Wideband CDMA transceivers often use direct IF sampling, meaning that the ADC samples signals with a 70MHz center frequency and 5MHz of bandwidth per channel. Up to 4 WCDMA channels are transmitted simultaneously, spaced closely in frequency. This places difficult intermodulation distortion (IMD) and noise requirements on the components in the transceiver, since both raise the noise floor in the closely spaced adjacent channels. The LT1993-2 boasts an exceptional –70dBc IMD and low noise, allowing 63dBc of adjacent channel leakage ratio (ACLR) for WCDMA signals. This figure exceeds most WCDMA manufacturers' ACLR specifications.

Figure 3 shows the LT1993-2 driving a LTC2255 14-bit ADC with a 70MHz, 4-channel WCDMA signal. On the output of the LT1993-2 is a simple LC bandpass filter that adds additional out-of-band filtering. Figure 4 shows the FFT data from the LTC2255, demonstrating the good ACLR possible with the LT1993-2. The small aberrations on the sides of the WCDMA signals are artifacts of a noisy signal generator, whose output was bandpass filtered prior to reaching the LT1993-2.

Conclusion

The LT1993-x is a flexible, cost saving, and easy-to-use differential amplifier and ADC driver that ensures the best performance in high speed communications transceiver applications. Besides the low noise, low distortion and high speed, the LT1993-x also saves space with its 0.8mm tall 3mm × 3mm QFN package. Minimal support circuitry is required to operate the LT1993-x under most conditions and output lowpass filtering is included. Three different gain options increase the flexibility of system design and help reduce the gain requirements of noisier system components. The LT1993-x can simplify transceiver designs, reduce component count and reduce product time-to-market.

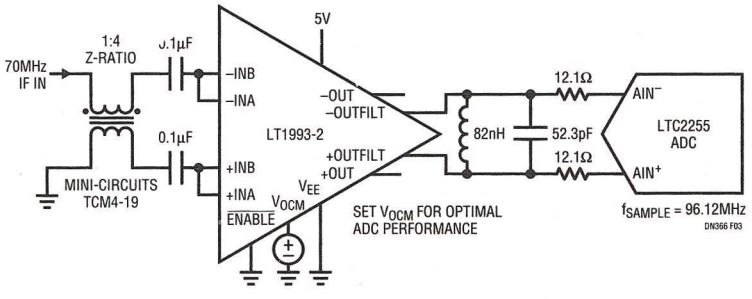

Figure 3. The LT1993-2 Driving an LTC2255 ADC Sampling at 96.12Msps with a 70MHz, 4-Channel WCDMA Signal. The Simple LC Output Network Provides Out-of-Band Filtering

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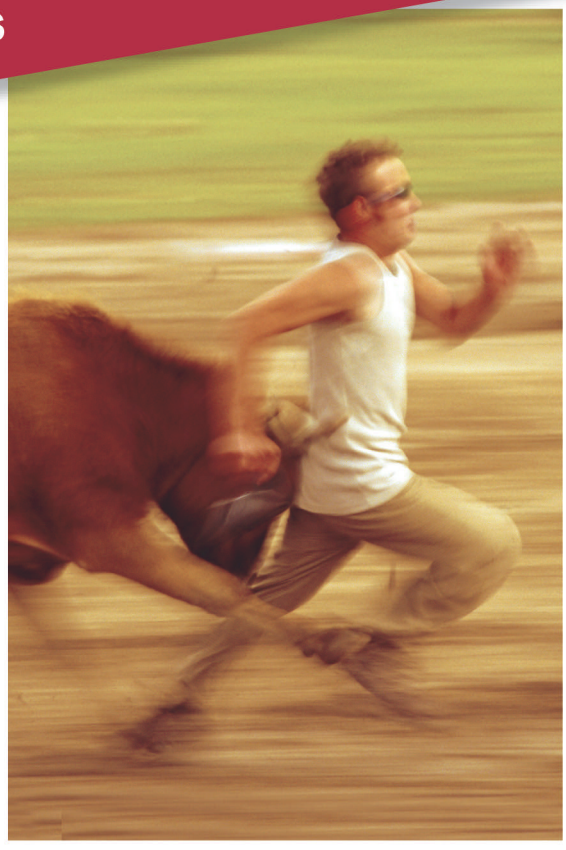

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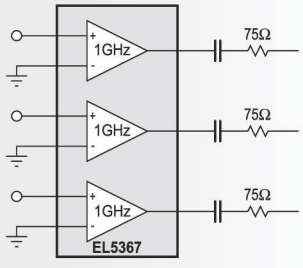

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EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
EL5367	1000	6000	8.5	1	160	±3.8

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Part No.	# of Amps	BW (MHz)	SR (V/µs)	IS (mA)	AV (min) (V)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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Part No.	# of Amps	BW (MHz)	SR (V/µs)	VN (nV/√ Hz)	IS (mA)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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A relatively large value of capacitance minimizes the negative-going ripple on V_{OUT}, which can be useful when dealing with low frequencies, low-duty-cycle pulse trains, or both. However, making C_1 too large renders the detector sluggish when responding to a sudden decrease in input-signal amplitude. Note that C_1 also affects the attack time; for example, doubling the capacitance doubles the time the circuit takes to acquire the peak level of V_{IN}.

Because the comparator's feedback path includes op amp IC_{2A}, offsets and errors that IC_{2A} presents have no effect on the circuit's accuracy. At low to moderate frequencies, only the comparator's input offset errors contribute to the detector's overall accuracy. At high frequencies, the comparator's response time becomes a significant factor, leading to a reduction in V_{OUT} that worsens as the frequency increases. Despite these limitations, the circuit performs well over several decades of frequency from approximately 50 Hz to 500 kHz. **Figure 2** and **Table 1** show the test circuit's sine-wave-frequency response by plotting the error in V_{OUT} for three peak levels of V_{IN}.

The oscilloscope photo shows the circuit's response to a 500-mV peak sine wave at 400 kHz, in which the output voltage, at 488 mV, lies just below the positive peaks (**Figure 3**). In addition to exhibiting good sine-wave response, the test circuit produces good results with rectangular signals of duty cycles as low as 5%. Note that the virtual ground at IC_{2A}'s inverting input restricts V_{OUT} to positive voltages only. Therefore, the circuit can respond only to true positive peaks—that is, peaks that go above 0V. If the input signal goes entirely below 0V, V_{OUT} simply levels off at 0V.

Although not essential to the circuit's operation, the lowpass filter and buffer formed by R_3, C_2, and IC_{2B} can minimize any switching noise that appears on V_{OUT}. However, offset errors inherent to op amp IC_{2B} affect the filter's output voltage.

Figure 4 shows a single-supply version of the circuit, in which R_A and R_B set a reference voltage, V_{REF}, at IC_{2A}'s

TABLE 1 SINE-WAVE-FREQUENCY RESPONSE

Frequency (Hz)	Error V_{IN}=2.5V peak (%)	Error V_{IN}=250 mV peak (%)	Error V_{IN}=25 mV peak (%)
200	−0.4	0.8	10
2000	−0.4	1.2	10
20,000	0	0.4	6.4
200,000	0	−2.4	−7.6
400,000	0	−4	−22
500,000	−2.4	−4.8	−28.4
600,000	−12	−6	−34

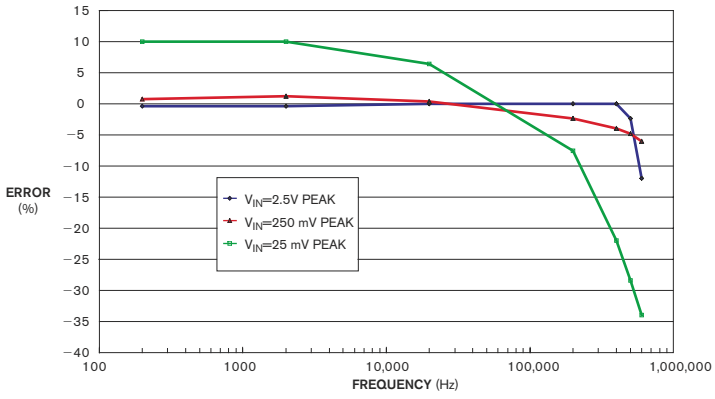

Figure 2 Plotting the difference between peak signal levels and output voltage for three peak levels illustrates the detector's frequency response.

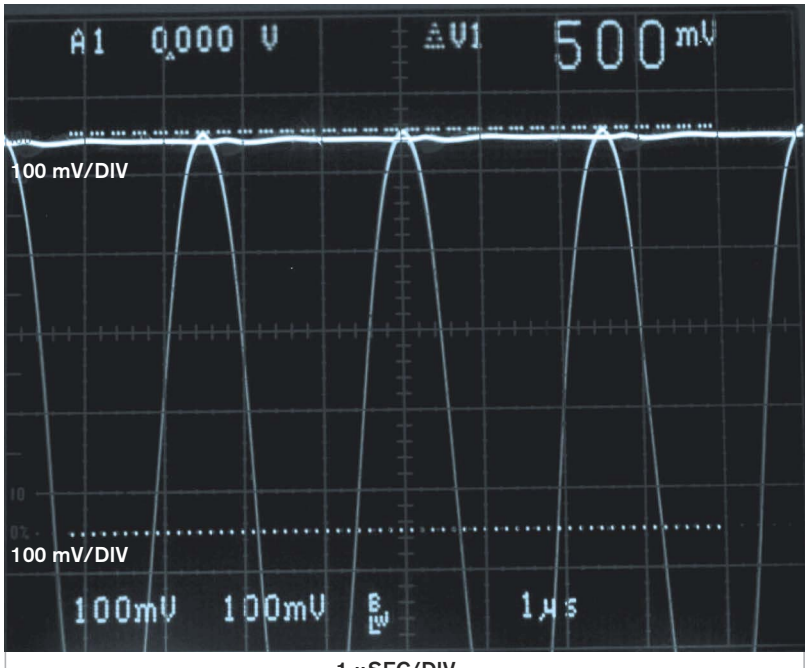

Figure 3 An oscilloscope photo displays input versus output voltages for a 400-kHz, 500-mV sine wave.

12-/8-/6-CHANNEL DS3/E3 ATM/PACKET PHYs SAVE SPACE

The DS31612 Is 15% Smaller than Competitive Solutions

The DS316x family of fully integrated DS3/E3 PHYs maps ATM cells and/or HDLC packets into DS3, E3, or 52Mbps clear-channel data streams. The DS31612 (12-channel), DS3168 (8-channel), and DS3166 (6-channel) devices are pin and software compatible for easy port-density migration on a single PCB design. To ease design upgrades, these devices are packaged with the same footprint as the earlier DS3164/3/2/1 (4-/3-/2-/1-port) ATM/packet PHYs.

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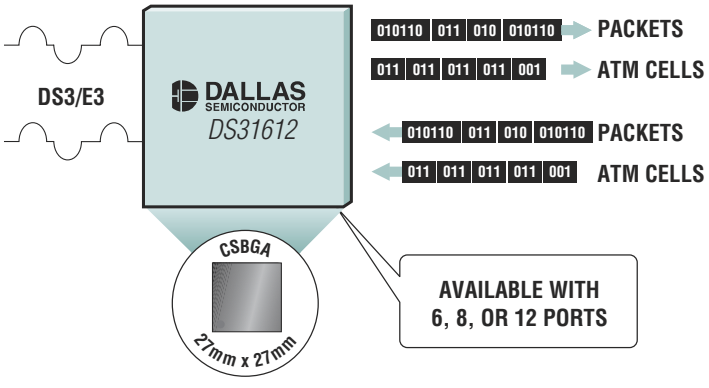

Part	Temp Range (°C)	No. of Ports	Package
DS31612	0 to +70	12	27mm² CSBGA
DS31612N	-40 to +85	12	27mm² CSBGA
DS3168	0 to +70	8	27mm² CSBGA
DS3168N	-40 to +85	8	27mm² CSBGA
DS3166	0 to +70	6	27mm² CSBGA
DS3166N	-40 to +85	6	27mm² CSBGA

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noninverting input, such that IC_{2A} maintains a virtual potential equal to V_{REF} at the inverting input. Thus, when V_{IN} goes more positive than V_{OUT}, the comparator's output MOSFET turns on, pulling the output down to 0V and impressing a potential equal to V_{REF} across R_1. This action, in turn, injects a current pulse equal to V_{REF}/R_1 into C_1. In most respects, the circuit behaves in the same manner as the circuit in **Figure 1**. As in the dual-rail version, V_{OUT} cannot go below the potential at the op amp's noninverting input. Therefore, even though V_{IN} need not center on a potential equal to V_{REF}, V_{IN}'s positive peaks must exceed V_{REF} for the circuit to work properly.

To select a value for V_{REF}, examine the input and output common-mode-voltage ranges of both op amp IC_{2A} and comparator IC_1 and the maximum peak-to-peak swing of the input signal. For example, setting the positive power-supply voltage, V_S, to 10V and setting $R_A=R_B$ sets $V_{REF}=5V$. The detector accommodates an input signal that swings from 0V to approximately 8V and thus detects positive peak voltages of 5 to 8V. Remember to select R_1 according to the value chosen for V_{REF}.EDN

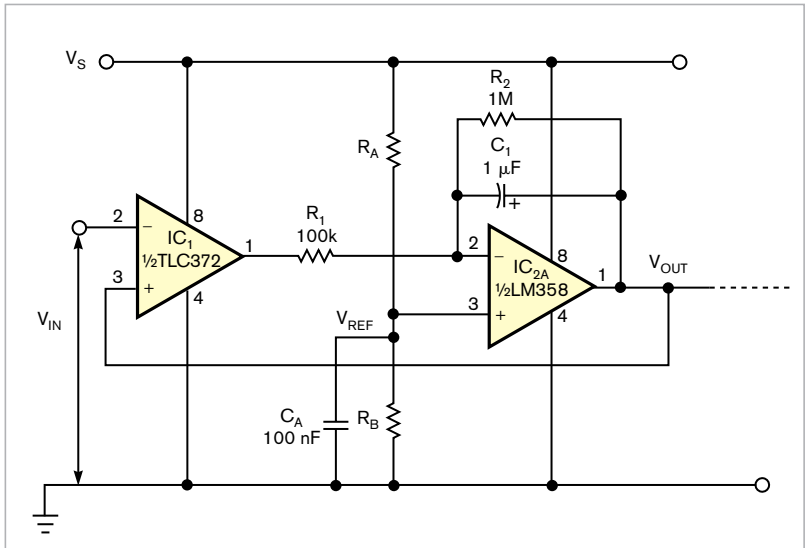

Figure 4 For operation from a single power supply, this version of the peak detector sets a reference voltage via resistors R_A and R_B.

Free program designs and analyzes passive and active filters

James Squire, Virginia Military Institute, Lexington, VA

At one time or another, most electrical engineers encounter a requirement to design or analyze an analog filter. Despite an abundance of graphical-user-interface-based digital-filter-design tools, such as The MathWorks (www.mathworks.com) Matlab Signals toolbox, which includes the FDATool filter-analysis package, few general-purpose, intuitive, and free GUI tools exist for synthesis of arbitrary active analog filters. To fill the need for a powerful and intuitive filter-design tool, this Design Idea describes an active-filter-design tool that bioengineering students at the Massachusetts Institute of Technology and at least four other universities use. Although originally implemented to run under Matlab, you can download a free copy of the program's stand-alone version at www.jamessquire.net. Select the "Research" menu and scroll to the software section at the bottom of the page. From the program list, select "Active Filter Design for Matlab" to download a copy of Filter Free 4.0.

Filter Free's functions include third-order analog and IIR (infinite-impulse-response) filters and 10-tap FIR (finite-impulse-response) filters. The program synthesizes filter designs and analyzes the frequency, time, and reflection responses of the ideal, unmodified filters. You can also view transfer functions in standard formats and pole-zero patterns. Using Filter Free, you can select any of 11 filter topologies ranging from gaussian to delay in bandstop, bandpass, highpass, and lowpass responses in five passive, transmission-line, active, switched-capacitor, and digital implementations.

As a design tool, Filter Free simulates a filter's frequency and time-domain responses as assembled using idealized component values. For component-approximation purposes, a round-off option reduces the number of significant figures in components' values. Data-display options include time or frequency response, pole-zero plots, transfer function, and reflection coefficient. You can select graphical plots' axis format, scale factors, and units of measurement.

As a teaching tool, Filter Free can load a user-supplied data file containing a stimulus waveform and simulate a filter's time- and frequency-domain responses. You can download 2000-point data files containing sample waveforms from www.nuhertz.com/filter/sampledata.html. Although the program's user interface is self-explanatory and includes built-in help menus, you can obtain a copy of the program's user's manual in Adobe's pdf format from the download site.EDN

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Contains RTC, Battery, and Crystal in a 11.8mm x 15.3mm Footprint

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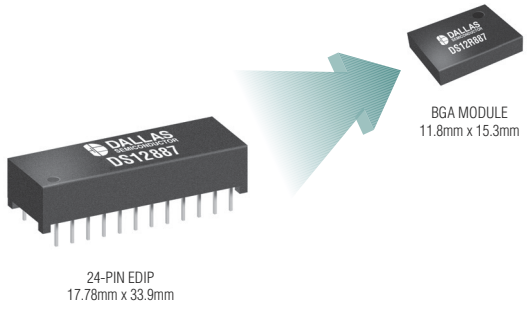

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Part	IR Reflow	Temperature Range (°C)	Voltage (V)	Pin-Package	Price† ($)
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DS12R887-5	Yes	-40 to +85	+5.0	48-Ball BGA	4.33

†1000-up recommended resale. Price provided is for design guidance and is FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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▷**Caddock Electronics Inc, www.caddock.com**

SMT drum-core power inductors meet UL94 standards

Five series of unshielded and shielded SMT drum-core power inductors comply with the guidelines of ROHS (restriction of hazardous substances) and UL94 V0 standards. Unshielded inductors are the 0.73×0.6×0.45-in. PF0504 series with 15 values from 0.68 µH/20A to 150 µH/2A, the 0.185×0.165×0.137-in. PF0580 series with 22 values from 1 µH/3.1A to 65 µH/0.41A, and the 0.406×0.367×0.174-in. PF0581 with 22 values from 10 µH/2.5A to 560 µH/0.32A. Shielded power inductors include the 0.272×0.256×0.118-in. PF0601 series with 22 values from 2.9 µH/2A to 330 µH/0.19A, and the 0.409×0.406×0.157-in. PF0560 series with 15 values from 1.5 µH/6.5A to 330 µH/0.52A. The drum-core series costs 10 to 20 cents.

▷**Pulse, www.pulseeng.com**

Capped resistors deliver lower overall board temperature

Delivering thermal compliance and isolation from pc boards, the SMC series "capped" resistors come in ratings as high as 2W. Capped ends provide an overall lower board temperature. SMC1 series resistors are rated for 1W at 70°C with resistance values of 0.1Ω to 1 MΩ; SMC2 series resistors are rated for 2W at 25°C with resistance values of 0.2Ω to 2.2 MΩ; both devices have tolerances of 61, 62, and 65%, which allow a closer thermal match to pc boards, improved airflow by slightly raising the device, and temperature coefficients of resistance as low as 625 ppm/°C. All devices are ROHS (restriction-of-hazardous-substances)-compliant and suit high-temperature soldering processes with operating-temperature ranges of −55 to +150°C. SMC series resistors cost 15 cents (5000).

▷**IRC Inc, www.irctt.com**

Variable-linearity coils suit CRT applications

The 8255 and 8256 pc-board-mounted, variable-linearity coils target applications with yoke-current requirements of 6 and 9A, respectively. Additional features include extended operation as fast as 90 kHz and a footprint of 20.32 mm in diameter and 33.02 mm in height, resulting in minimal pc-board real-estate use. The products' price ranges from $4.37 to $4.63 based on quantities.

▷**Prem Magnetics Inc, www.premmagnetics.com**

Small transformers target DSL equipment

Suited for DSL equipment, Series B78416 interface transformers with an EP5XL core are 25% smaller, 31% lower, and 48% lower in volume than the EP7-based transformer. The devices have the same longitudinal balance and total-harmonic-distortion values as the EP7, with higher ohmic resistance, and they satisfy

leakage-inductance requirements. The transformers also satisfy requirements for surge-voltage strength.
▷**Epcos Inc, www.epcos.com**

High-current inductors have self-shielding design

Part of the Toroid Terminator family, the HM55A Series has a self-shielding molded-inductor design, delivering as much as 40A rated current, and

has an operating-temperature range as high as 155°C. Designed as a replacement for conventional bulky toroids, the series is available in 16×10×9- and 16×10×11.5-mm cases. Inductance values range from 0.28 to 2 µH, and the devices have a dc resistance of 0.72 mΩ±5%. The devices cost 28 cents each.
▷**BI Technologies, www.bitechnologies.com**

Passivated film resistor targets moisture-sensitive applications

A proprietary passivation layer between the Nichrome resistive element and the epoxy overcoat allows the RNCS series of anticorrosive precision chip resistors to operate in harsh and wet environments. The line comes in 0402 to 2512 sizes, has a resistance range of 4.7Ω to 1 MΩ with tolerances of ±0.01%, has temperature coefficients of resistance of 5 ppm/°C, and has an operating-temperature range of −55 to +150°C. The resistors cost 20 cents (1000).
▷**Stackpole Electronics, www.seielect.com**

Microminiature chip inductors have high Q value

PM0402T and PM0603T microminiature-chip-inductor series measure 1×0.5×0.35 mm and 1.6×0.8×0.45 mm, respectively. Features include an inductance range of 1 to 68 µH at 100 MHz, a Q value of 17 at 300 MHz, a minimum self-resonating frequency as high as 6 GHz, and a dc-current range of 70 to 800 mA. The PM0402T series costs 11.3 cents each, and the PM0603T series costs 18.3 cents each.
▷**JW Miller Magnetics, www.jwmiller.com**

(continued on pg 98)

PASSIVES

EMI filter has UL94 VO enclosure

These compact EMI filters come in an UL94 VO plastic enclosure and are available for 100 to 120 or 200 to 240V line voltages. Standard models feature 5-mH common-mode inductors suitable for as much as 6A service. The devices cost $3 (1000).

▷**Foster Transformers, www.foster-transformer.com**

Ceramic capacitors reduce short-circuit risk

Targeting automotive electronic circuits, series B37941X capacitors suit applications with capacitors permanently connecting to the positive pole without extra safety measures. Rated at 100 and 50V, they feature a capacitance range from 1 to 100 nF and 33 to 100 nF, respectively. The capacitors conform to AECQ200 standards and come in size 0805 and ceramic material X7R.

▷**Epcos Inc, www.epcos.com**

INTEGRATED CIRCUITS

Dual-channel video-format converter renders side-by-side high-quality images

The AVC5000 dual-channel video-format converter features two high-quality video-conversion channels and dual 3-D architecture. It enables picture-in-picture rendering of two images on a wide-screen HDTV with a 1080-pixel line-progression display resolution. The universal front end accepts standard- and high-definition video, PC-graphics formats, and DVI signals and decodes them into component video or RGB. The converter includes seven ADCs, a TMDS receiver, and two NTSC/PAL/SECAM decoders with 3-D Y/C separation. The dual-channel display processor features two 3-D noise reducers, two 3-D deinterlacers, and two high-order scalers for size and aspect-ratio scaling. Additional features include luma and chroma enhancement, frame-rate conversion, adaptive contrast enhancement, intelligent color remapping, and generation and overlay of bit-mapped OSD. Packaged in a BGA-544, the AVC5000 costs $125 each (1000).

▷**National Semiconductor, www.national.com**

Storage-chip portfolio has hard-coded TMA

The NASn01 (network-attached-storage, in which n stands for the number of SATA 1 hard-disk drives the chips can support) series includes the NAS8xx, NAS4xx, NAS2xx, and NAS-1xx. Featuring content protection through RAID 0, 1, 4, and 5; multiple hard-disk-drive configurations of one, two, four, and eight; and optional data security, the chips also have gigabit Ethernet and USB 2.0 interfaces. Hard-coded in the chips is a TMA (traffic-management-arbitrator) block that schedules, controls, and delivers stream-aware quality-of-service management, allowing non-blocking, bidirectional 1-Gbyte throughput. The chips cost $36 (1000).

▷**Agere Systems, www.agere.com**

Codec simultaneously runs ADC and DAC

As a single-ended-input, two-wire control version of the WM8590, the WM8591 stereo-audio codec can simultaneously operate the ADC and DAC at different sample rates. Available now for sampling, the codec costs $1.45 (10,000).

▷**Wolfson Microelectronics, www.wolfsonmicro.com**

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The WiMax simulation testbench simulates subscriber transmissions; developers can use it alongside Aspex's 802.16d/e PHY (physical-layer) baseband architecture. The software is written in Matlab and meets Aspex's reference code for implementing multiantenna base stations.

▷**Cambridge Consultants, www.cambridgeconsultants.com**

Mixed-signal-IC family suits LCD-TV applications

The single-chip VCT 69xyP family of pin- and software-compatible ICs features a 3-D comb filter, a component input for HDTV signals, LVDS outputs, European HD-Ready label for WXGA FPD-TVs through a 24-bit RGB interface, and an I²S audio input connected to an external DVI- or HDMI-receiver IC. The devices include a separate headphone channel and a five-band equalizer, and Virtual Dolby Surround, BBE, and SRS TruSurround XT are optional. The Eco Version suits smaller LCD-TV requirements with a 2-D-color decoder, line-based deinterlacer, and 10 pages of teletext; the basic version suits midsized LCD panels with a motion-adaptive frame-based deinterlacer and 500 pages of teletext; and the premium version features a 3-D-color decoder, a motion-adaptive frame-based deinterlacer, and 1000 pages of teletext. The VCT 69xyP comes in an LQFP-208 package and requires no additional external RAM or flash.

▷**Micronas, www.micronas.com**

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STATS Introduced in 2003 / More than 1.2 million sold / Cost: $199

Robot vacuum cleaner cleans up in many ways

Labor-saving home appliances are the stuff of fact (think clothes washers and dryers) and fiction (think "The Jetsons"), but sophisticated home robots have had a difficult time in the market, due to their cost, performance, and maintenance issues, when compared with the benefits they actually yield. That frustrating situation changed in 2003, when iRobot Corp (www.irobot.com) introduced the one-function Roomba robot vacuum. Although primarily a designer and manufacturer of military and industrial-exploration robots, the company has through various mass-distribution channels sold more than 1.2 million units of the $199 Roomba, which has spawned several competitors and imitators.

The Roomba is made possible by a clever design that combines low-cost sensors, a 16-bit microcontroller, flash memory, a multithreaded operating system, an efficient motor and drive, and advances in battery technology, all of which pack into the disk-shaped unit. The next step? On May 25, 2005, the company announced the Scooba, a robotic floor-mopping unit that it plans for retail sale early in 2006. It vacuums loose debris, squirts down a special cleaning fluid from Clorox, and squeegees up the dirty water.—by Bill Schweber, Executive Editor

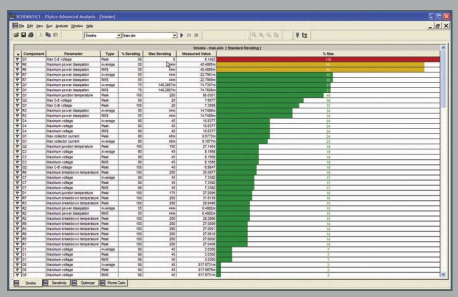
COURTESY OF IROBOT

Can you find the problem on this board? Can your design software?

PSpice now offers advanced stress analysis capabilities to help you catch problems before they happen

The PSpice® Smoke Option can help warn you of component stress due to power dissipation, increases in junction temperature, secondary breakdowns, or violations of voltage/current limits. The PSpice Smoke Option compares circuit simulation results to the component's safe operating limits defined by the manufacturers. If limits are exceeded, the PSpice Smoke Option identifies the problem parts and the limits exceeded.

The PSpice Smoke Option is ideal for displaying average, RMS, or peak values from simulation results and comparing these values against corresponding safe operating limits. You can even derate manufacturers' limits to build in a margin of safety for your design.



Use the PSpice Smoke Option to Identify Components Exceeding Manufacturers' Limits

- Maximum current limits
- Power dissipation for each component
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- Junction temperatures
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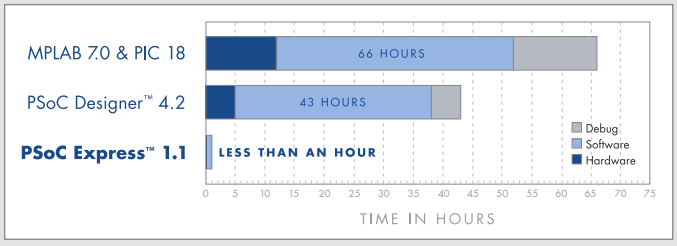

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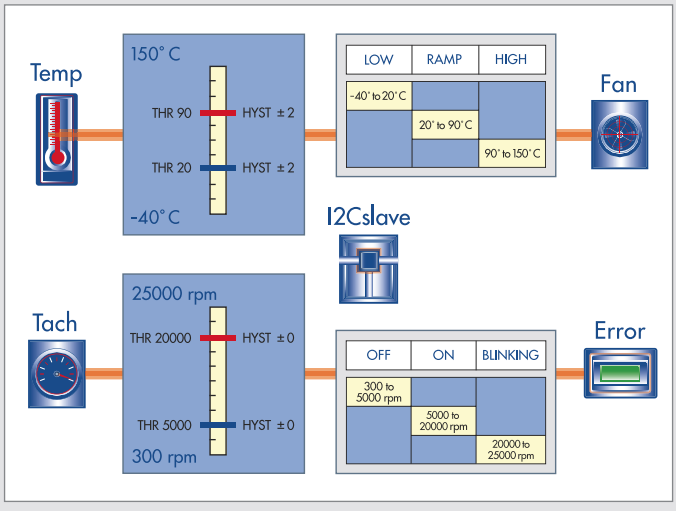

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